PERFORMANCE ANALYSIS OF NEXT GENERATION GRAPHENE INTERCONNECTS

by

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Declaration

I hereby declare that

i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology and has not been submitted elsewhere for a degree,

ii) due acknowledgment has been made in the text to all the reference material used.

Nikita Patel

Certificate

This is to certify that the thesis work entitled PERFORMANCE ANALYSIS OF NEXT GENERATION GRAPHENE INTERCONNECTS has been carried out by Nikita Patel for the degree of Master of Technology in Information and Communication Technology at *Dhirubhai Ambani Institute of Information and Communication Technology* under my supervision.

Dr. Yash Agrawal
Thesis Supervisor

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Contents

Abstract

The state-of-the-art development and subsequent miniaturization of technologies in e-systems such as computers and digital communication systems, have led to densely and compactly placement of devices and interconnects in ICs. The incessant advancements of technologies have necessitated a rapid increase in operating frequencies. At nanometer dimensions and advanced technology nodes, performance of the overall VLSI system is critically dominated by on-chip interconnects.

Interconnects perpetuate several non-ideal effects such as signal delay, power dissipation and crosstalk that limit the overall system performance. Owing to graving effect of interconnects on the performance parameters in ICs, research into interconnects has become meticulously very active in recent years, and concurrently much progress has been made. In the present work contemporary advancements on conventional aluminum, copper and subsequent performance analysis of next-generation graphene interconnects have been systematically performed.

In compact and portable e-systems, demand for ultra low power applications has become very high. Subthreshold region of operation is one of the most efficient techniques to attain low power in circuits and systems. The performance of graphene interconnects at subthreshold region and its future scope have been meticulously explored in the present work.

The advanced graphene on-chip interconnects have been considered for the performance analysis. The technology node considered is 22nm. It is analyzed that graphene based MLGNR interconnects possess better performance over copper interconnects. It is also seen that subthreshold region of operation leads to significant lower power dissipation than in linear region. Power saving with subthreshold region of operation in case of conventional copper and advanced graphene interconnects are nearly 22% and 26% respectively. The various proposed FDTD modeling for subthreshold region is highly accurate with respect to SPICE simulation results. The maximum percentage error is less than 3%.

At miniaturized technology nodes, variation due to temperature, fabrication process and environmental fluctuations crops up significantly that varies the system output in on-chip ICs. As a result, variability analysis of on-chip interconnects at nano regime in subthreshold region has become need of the hour. Variability analysis of graphene interconnect in subthreshold region is presented. Process corner, parametric and Monte-Carlo analyses have been performed to determine variability effect in on-chip multilayer graphene nanoribbon (MLGNR) interconnects.

List of Symbols

C	Capacitance
C_D	Depletion capacitance
C_{OX}	Oxide capacitance
d	Diameter
e	Electronic charge
h	Height
$H(s)$	Transfer function
I	Current
K	Total no of points along space
L	Inductance
l	Length
m_i	Taylor's series coefficient
n	Chiral index of CNT
N	Total no of points in time domain
η	Subthreshold slope
N_{ch}	Number of conducting channel in MLGNR
N_{layer}	Number of layers in MLGNR
R	Resistance
t	Time
T	Thickness
T_{OX}	Oxide thickness
V	Voltage
V_{ds}	Drain to source voltage of transistor
V_{DD}	Supply voltage at drain terminal of transistor
v_F	Fermi velocity
V_{gs}	Gate to source voltage of transistor
V_T	Thermal Voltage
V_{th}	Threshold voltage of transistor

w	Width
x	Distance
μ	Mobility
Δ	Small difference
δ	Vander Waals gap
λ	Mean free path
ρ	Resistivity
ψ	Angle of rotation in CNT
$\hbar$	Planck's constant

List of Acronyms

ac-GNR	armchair Graphene Nano Ribbon
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
DIL	Driver Interconnect Load
DSM	Deep Sub Micron
FDTD	Finite-Difference Time-Domain
FET	Field Effect Transistor
GNR	Graphene Nano Ribbon
ICs	Integrated Circuits
MLGNR	Multi Layer Graphene Nano Ribbon
MWCNT	Multi Wall Carbon Nanotube
PDF	Probability Distribution Function
PDP	Power Delay Product
SC-GNR	Side Contact GNR
SLGNR	Single Layer Graphene Nano Ribbon
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Wall Carbon Nanotube
TC-GNR	Top Contact GNR
VLSI	Very Large Scale Integration
zz-GNR	zigzag Graphene Nano Ribbon

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CHAPTER 1
Introduction and Problem Formulation

1.1 Introduction

In very-large-scale integrated (VLSI) circuits, millions of devices and transistors are integrated on a single chip. As technology scales down, interconnects start playing dominant role in determining overall performance. At small technology nodes overall system performance degrades due to parasitic effects of interconnect. Interconnect parasitic elements are capacitance, resistance and inductance. These causes delay, power dissipation and cross talk in ICs. On-chip interconnects have thus become a major concerning factor and very important research topic.
Based on the dimensions of wire, on-chip interconnects are categorized as: local, intermediate and global. Local interconnects have very thin lines and are used to connect gates and transistors within a unit or in a functional block of the chip. Typical length of local interconnects is a few micrometers. Intermediate wires are thicker and used to provide comparatively lower resistance to signal/clock paths. Typical length is in the range of tens of micrometers. Distribution of clock and signal between the functional block is done using global interconnections. These wires occupy top one or two layers of interconnections [1].
Till date several materials have been employed for on-chip interconnects in ICs. Metallic wires namely aluminum (Al) and copper (Cu) have been widely used for interconnections in ICs [1]. Al had been used to form metallic interconnects in ICs because of its low resistivity and silicon compatibility. As device dimensions reduce, current density increases. Further at nano dimensions, reliability of VLSI circuit reduces. This is due to electro-migration effects and electrical shorts that create tunnel between successive levels of Al [2]. Thus at scaled dimensions Al cannot be used for on-chip interconnect application. Other potential metallic conductors with lower electrical resistivity lower than aluminum are gold, silver and copper. Cu with close to half the resistivity of Al shows nearly ten times better performance in terms of lower electro-migration effects [1]. Thus, Cu has

been one of the most appropriate materials and desired choice for VLSI interconnects in ICs [1]. Tungsten has also been used for high-end applications. To reduce electro-migration issues, two or more metal layers have also been used for interconnections in ICs. A few of the multilayer interconnections materials are Al/Cu, Al/Ti/Cu, Al/Ta/Al, Al/Ni, Al/Cr, Al/Mg, and Al/Ti/Si [2]. Graphene is alternative potential new material used in interconnects which has several advantages over other metallic materials. Graphene is the one of the forms of carbon. Graphene has two different structures CNT (carbon nanotube) and GNR (graphene nanoribbon) which are briefly discussed in section 2.2. For ultra low power circuit designs, high power dissipation is a major concern in application such as internet of Things (IOT) enabled devices and portable devices. Several researches have been performed to attain low power dissipation in ICs. Subthreshold region of operation satisfies ultra low power requirement and consequently has gained much research attention recently. Circuit operations on subthreshold region consume less energy. However, this improvement comes at the cost of slow performance. So, its application is limited to certain area where power is the major concern [3].

1.2 Motivation

Presently Cu is most widely used material for on-chip interconnects. The resistivity of Cu interconnects increases rapidly because of the effects of enhanced gain surface scattering, longer interconnect length, higher operating frequency and Joule heating. Increased heating and high temperature further stimulates electromigration induced hillocks and voids. These cumulatively limit the performance and cause signal integrity, skin effect, higher power dissipation and crosstalk in ICs. As a result, there is need for alternative prospective material for on-chip interconnect applications [1], [4].

As device density in ICs increase, power dissipation also increases tremendously. Further, portable e-gadgets demand low power techniques for high-end performance. VLSI designers have searched for several different materials and their fabrication methods that can be potentially used in the upcoming years. Graphene, silicon and metal nanowires, optical interconnects have been explored to be prospective interconnection materials for advanced technology nodes [4].

1.3 Problem formulation

To investigate the performance of graphene interconnects in subthreshold region of operation using mathematical model. Graphene derived multilayer graphene nanoribbon (MLGNR) interconnect is considered for the performance analysis. The analytical mathematical model is based on numerical method based finite-difference time-domain (FDTD) technique. MLGNR interconnect are modeled using FDTD model and compared with SPICE results.

1.4 Objectives

Scaling of ICs leads to many signal integrity issues. The demands of higher speed, higher operational frequency, lower power dissipation and smaller chip size have made on-chip interconnects very important research topic. Copper will no more work for interconnection at nanodimensions and henceforth the prospective solution to mitigate this is to have interconnect material such as carbon nanotubes (CNTs) and graphene nanoribbons (GNRs).
Further need of low power applications for IOT, wireless sensor network (WSN) and other applications is high on demand. Subthreshold circuit of operation gives advantage of lower power dissipation and is the potential solution for the ultra low power requirement. Subthreshold region of operation with graphene interconnect is new topic of research.
The proposed objectives to accomplish the above goals are detailed as follows:

1. To review the various copper and graphene on-chip interconnect structures and their modeling techniques.

2. Performance analysis of graphene interconnects using finite difference time domain (FDTD) model.

3. Investigation of graphene interconnects in subthreshold region using FDTD model.

4. Variability analysis of graphene interconnects in subthreshold region.

1.5 Organization of thesis

This thesis consists of the 8 chapters to attain the solution of the problems defined in the objectives. Present chapter represents the introduction and problem formulation. Next chapter is the literature review of the topic. It details about different electrical wire models viz. lumped, distributed and transmission line. Then the graphene interconnects have been discussed. At last, subthreshold region of operation and its modeling part have been detailed in this chapter. Chapter 3 details about the performance improvement techniques of on-chip interconnect viz. wire engineering, shielding, repeater insertion, methods of signaling and interconnect material. The mathematical modeling techniques to analyze interconnects are detailed in chapter 4. The different mathematical models discussed are moment matching technique, two-port network and numerical method analysis based FDTD technique. In chapter 5, formulations to extract the parasitics of copper, CNT and MLGNR interconnect have been defined. Performance analysis of graphene interconnect in subthreshold region of operation using proposed FDTD model is presented in chapter 6. The variability analysis of graphene interconnect is presented in chapter 7. Finally conclusion is drawn in chapter 8.

CHAPTER 2
Literature Review on On-chip Interconnect

In this chapter, basics of interconnect and their electrical wire modeling have been presented. Further, graphene derived CNT and GNR structure and their physical characteristics are discussed. Also various work performed in subthreshold region of operation have been discussed.

2.1 Electrical wire models of interconnect

Performance analysis of copper and aluminum interconnect have been performed by various researchers [5-7]. In [5], void formation due to stress in aluminum interconnect is presented. It states that aluminum is major concerning problem for VLSI circuit. Failing of aluminum interconnect and consequently copper as a new interconnect material is introduced in [6]. It details about the advantages of copper interconnect over aluminum interconnect. Electro-migration effects of copper interconnect at nanodimensions is presented in [7]. It is investigated that copper interconnects have limited significance at nanoscale dimensions [8]. To mitigate these issues, graphene based interconnect have been identified as a potential solution to attain high performance in ICs. The parasitic elements of interconnect have impact on the electrical behavior of the circuit like circuit delay, power dissipation and reliability. For better understanding and analysis, electrical modeling of interconnects that estimate and approximate the real behavior of the wire is needed. The rest of this section details about the different interconnects models.

2.1.1 The lumped model of interconnect

The circuit parasitics of a wire in general are distributed along its length. It is generally not lumped into a single position. However, at low frequencies and short wire lengths, consideration of only lumped capacitive and resistive components of the wire is sufficient to capture the electrical characterization of the wire. This is shown in Figure 2.1, where l represents the total length of the wire, R and C are

the resistance and capacitance per unit length respectively. The interconnect can be treated as a lumped element. It can be represented by a low-pass *RC* segment. This model is incorporated when the physical dimension of an interconnect is much smaller than the wavelength of the signal passing through the interconnect. The advantage of doing this is that the effect of the parasitics can be described by an ordinary differential equations [9-10].

The lumped model can be configured in three different ways as L-model, π -model and T-model. These are represented in Figure 2.2.

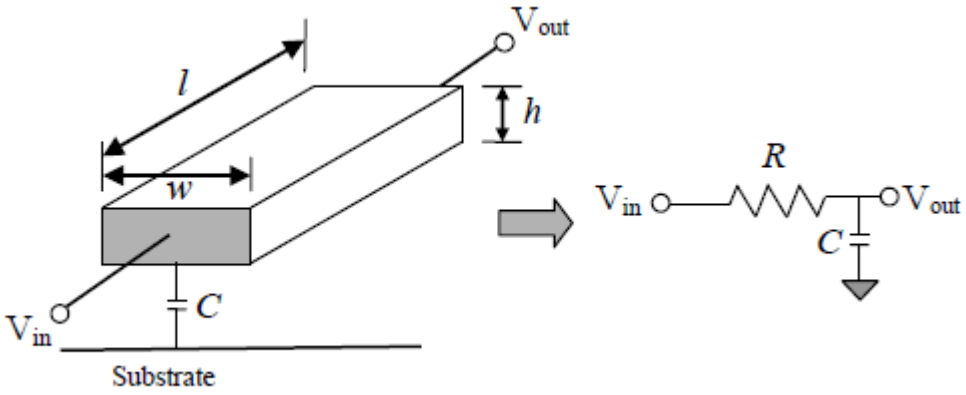

Figure 2.1: Lumped *RC* model of interconnects.

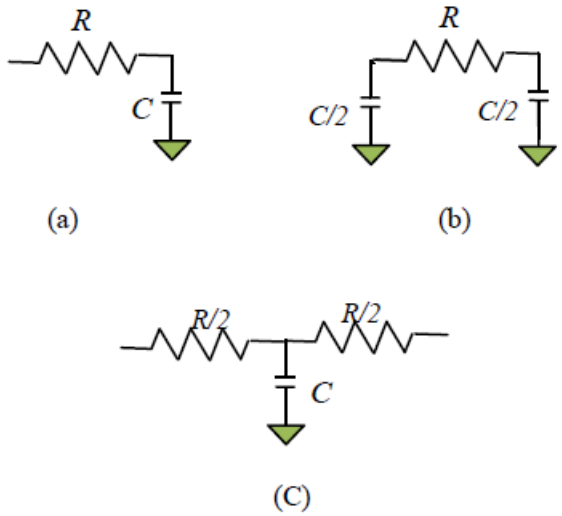

Figure 2.2: (a) L-model (b) π-model (c) T-model.

2.1.2 Distributed *RC* model of interconnect

Distributed *RC* model is more appropriate and accurate than lumped model. For long interconnects, when the physical dimensions of interconnect are in the range of the wave length of the signal passing through the interconnect, lumped model become inefficient. Henceforth, distributed model is used, as given in Figure 2.3. In Figure 2.3, v_i represents the voltage at node i.

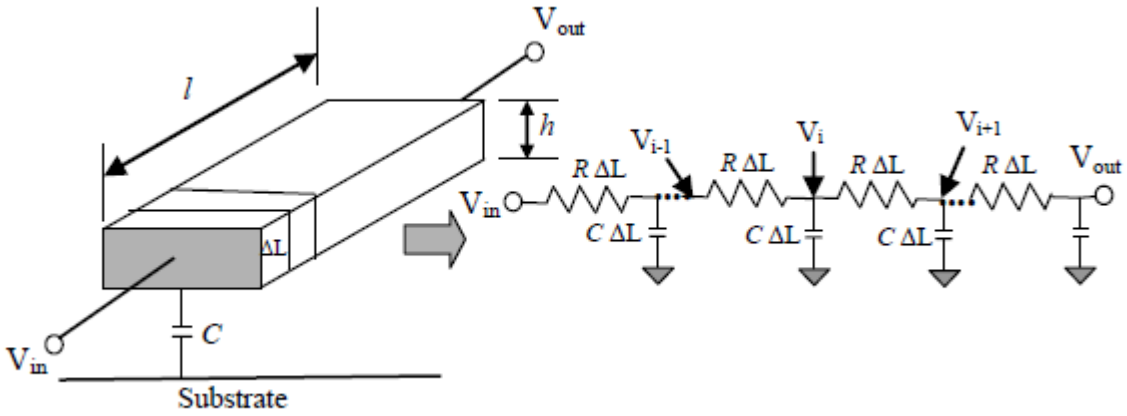

Figure 2.3: Distributed *RC* model of interconnect.

The mathematical formulation for distributed model can be obtained by applying Kirchhoff′s current and voltage (KCL and KVL) equations. Applying KCL at node i in Figure 2.3 gives,

$$\frac{v_i - v_{i-1}}{R(\Delta L)} + \frac{v_i - v_{i-1}}{R(\Delta L)} + C(\Delta L)\frac{dv_i}{dt} = 0 \tag{2.1}$$

This results,

$$RC\frac{dv_i}{dt} = \frac{(v_{i+1} - v_i) - (v_i - v_{i-1})}{(\Delta L)^2} \tag{2.2}$$

Let $\Delta v_{i+1} = (v_{i+1} - v_i), \Delta v_i = (v_i - v_{i-1})$, and taking the limit $\Delta l \to 0$, the diffusion equation of the distributed *RC* model of interconnects is solved. These gives solution in time domain as [9-10]:

$$RC\frac{\partial v_i}{\partial t} = \frac{\partial^2 v_i}{\partial x^2} \tag{2.3}$$

2.1.3 Transmission line model of interconnect

In transmission line model, parasitic inductance is also considered. Distributed *RLC* model also known as transmission line model is most accurate for the behav-

ior and characterization of interconnects. The transmission line model is shown in Figure 2.4. This model is important at high frequencies since at high frequencies incorporation of inductance becomes important. The transmission line has the prime property that signals propagate over the interconnection medium as wave which is not the case in distributed *RC* model. In this model, signal propagation is governed by the diffusion equation as stated in Equation (2.4). The signal propagates in transmission line model by transferring energy from the electric field to the magnetic field alternatively, or equivalently from the capacitive to the inductive modes. The governing equation in transmission line model is given as [9-10]:

$$\frac{\partial^2 v}{\partial x^2} = RC\frac{\partial v}{\partial t} + LC\frac{\partial^2 v}{\partial t^2} \tag{2.4}$$

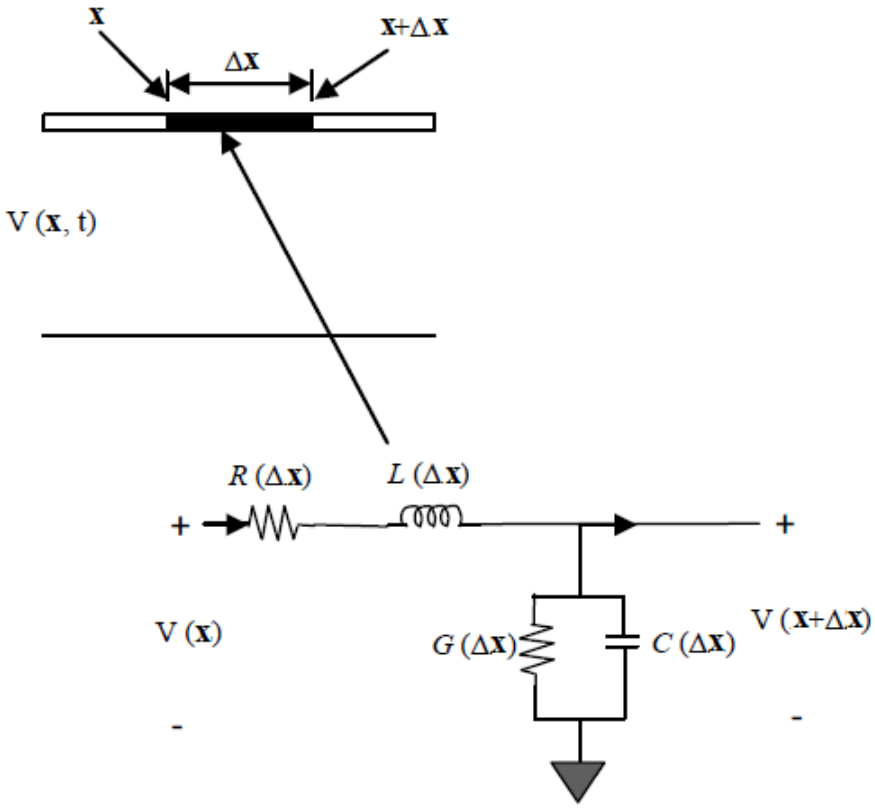

Figure 2.4: Lumped network model of an infinitesimal small section of transmission line.

2.2 Graphene interconnect

Carbon, the elementary constituent of graphite and graphene, its atomic number is six. Carbon is capable of forming many allotropes due to its ability to form bonds by mixing different orbitals namely s and p. The mass number (i.e. no. of protons + no. of neutrons) varies as 12, 13, 14 depending on the varying number of neutrons. Carbon exists in different isotopic forms as ${}^{12}_{6}C$, ${}^{13}_{6}C$, ${}^{14}_{6}C$. Isotope ${}^{12}_{6}C$ and ${}^{13}_{6}C$ are stable while ${}^{14}_{6}C$ is radioactive [11-12].
The lattice structure of graphene in real space consists of hexagonal arrangement of carbon atoms and is shown in Figure 2.5(a). The band structure of graphene is shown in Figure 2.5(b) [11-12].

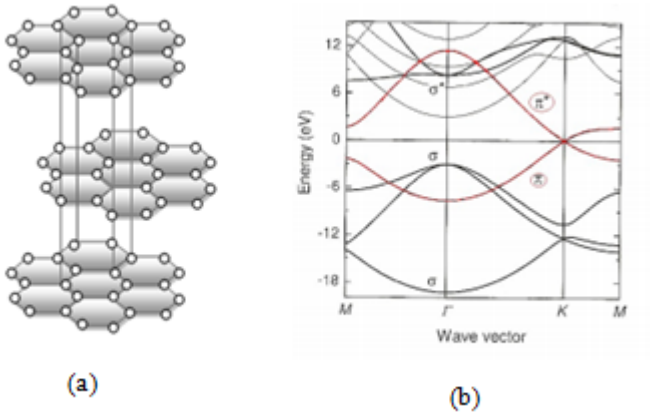

Figure 2.5: (a) Crystal structure (b) band structure of graphite [11-12].

CNTs and GNRs possess substantial higher electrical and mechanical properties than the conventional Al and Cu interconnects. The comparison of different interconnect materials are tabulated in Table 2.1.

Graphene is aptly suited in monolithic IC designs as this can be used to make both transistors and interconnects. Carbon allotrope graphene has been envisaged in high speed interconnects in ICs and have led to lots of research interests in the area of transistors and interconnects [13-16]. Carbon forms different hybridization as shown in Figure 2.6. [13], [17]. The bonds between atoms in graphene are stronger than in diamond that makes graphene as one of the strongest material [1].
In on-chip interconnects in ICs, graphene can be broadly of two types viz. CNT and GNR. These are discussed as follows:

Table 2.1: Properties of different on-chip interconnect materials [13]

Property	Al	Cu	SWCNT	MWCNT	MLGNR
Max current Density	10^6	10^7	$> 10^9$	$> 10^8$	$> 10^9$
Melting point (K)	933.5	1357	3800	3945	4900
Density (g/cm^3)	2.7	8.94	1.75-2.1	2.09-2.33	1.3-1.4
Conductivity ($\times 10^3$)W/mk	0.126	0.393	3	3-5	1.75-5.8
Temp-coeff ($\times 10^3$)K	4.3	4	-1.37	-1.47	<1.1
Mean free path at 300k (nm)	18	40	2.4×10^4	10^3	10^3

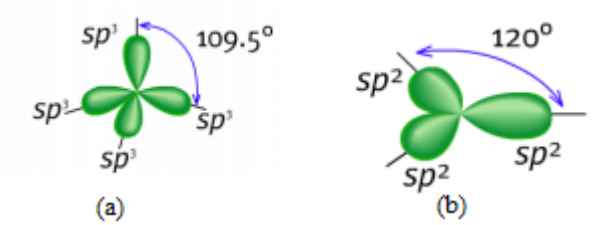

Figure 2.6: (a) sp^3 hybridization (b) sp^2 hybridization.

Carbon Nanotube (CNT)

Carbon nanotubes are made by rolling up sheet of graphene into a cylinder. These structures can be constructed with the length-to-diameter ratio of up to (1.32×10^8):1 [13]. The diameter of carbon nanotube is in the order of a few nanometers. In the field of nanoelectronics and interconnect applications, CNTs are one of the most promising candidate for high performance applications [18].

Based on chirality (the direction in which graphene is rolled), CNTs can be classified as armchair or zigzag. The schematic of armchair and zigzag are shown in Figure 2.7 [19]. The arrows in Figure 2.7 show the circumferential vector and the direction indicates the rolled-up direction of CNT. The diameter (d) and angle of rotation of CNT (Ψ) is computed as [13, 20]:

$$d = \frac{|C|}{\Pi} = \frac{a}{\Pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{2.5}$$

$$\Psi = \cos^{-1}\left(\frac{(n_1 + n_2)}{2\sqrt{{n_1}^2 + n_1 n_2 + {n_2}^2}}\right) \tag{2.6}$$

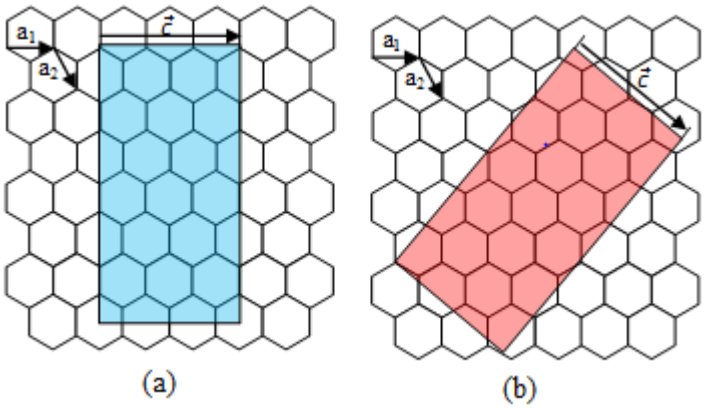

Figure 2.7: (a) Armchair (b) zigzag configuration of graphene [18].

The vector (c) is defined as $a_1n_1 + a_2n_2$, where a_1 and a_2 are the lattice vectors of graphene and n_1 and n_2 are the chiral indices. CNTs are an optimum solution for interconnects as its unique atomic arrangement and band structure give excellent electrical and mechanical properties. CNTs can be categorized into single wall carbon nanotube (SWCNT) and multiwall carbon nanotube (MWCNT). These are shown in Figure 2.8.

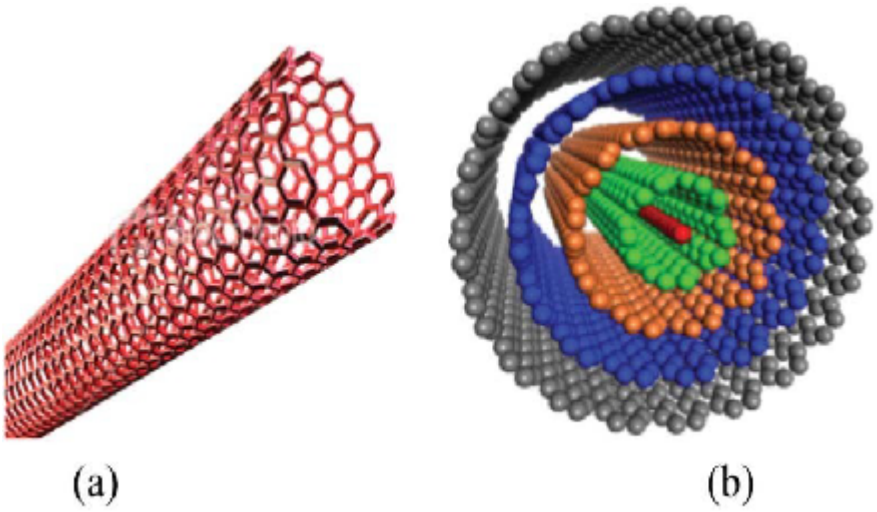

Figure 2.8: Graphene derived (a) SWCNT (b) MWCNT structure [18].

CNTs can be either metallic or semiconductive in nature, depending on the chirality or rolling angle [19]. Metallic CNTs are more desirable because it gives advantage of seamless charge carriers movement across the devices for on-chip interconnects applications. SWCNTs comprise of single rolled up graphene sheet. The DC resistance of isolated SWCNT is very high. Hence, bundle structure of

SWCNT is used. It is analyzed that CNT bundle structure can have signified higher performance over Cu interconnects [1]. MWCNT comprises of concentric shells of graphene. MWCNTs are always metallic because of large diameter of shells [21]. The performance analyses of bundled structure of MWCNTs have also been analyzed in [19, 22]. MWCNT bundle with large diameter and in proper contact can reduce interconnect parasitic considerably. This results in higher current conduction and conducting channels that consequences better performance than isolated MWCNT, SWCNT bundle and copper interconnects [19, 23].

Graphene Nano Ribbon (GNR)

Graphene nanoribbons are strips of graphene of width lesser than about 50nm [20]. Depending on the orientation of graphene sheet, GNR can be either armchair GNR (ac-GNR) or zigzag GNR (zz-GNR). Zigzag GNR is always metallic whereas armchair GNR can be metallic or semi-conducting [20]. The metallic or semiconductive nature of ac-GNRs is determined from the number of hexagonal rings (N) across the width of GNR. In metallic ac-GNRs, $N = 3p - 1$ or $3p + 2$, whereas $N = 3p$ or $3p + 1$ for semi-conducting GNR, where p is any integer. Owing to aptly suited electrical and thermal properties, it is important to understand the electronic band structure of graphene. The band structure of graphene is obtained using tight binding approximation [24]. Figure 2.9 shows the band structure of metallic ac-GNR and semiconducting ac-GNR. In metallic ac-GNR, there is a slight overlapping of bands as shown in Figure 2.9(a), whereas in semiconducting ac-GNR, there exists bandgap and is shown Figure 2.9(b) [25].

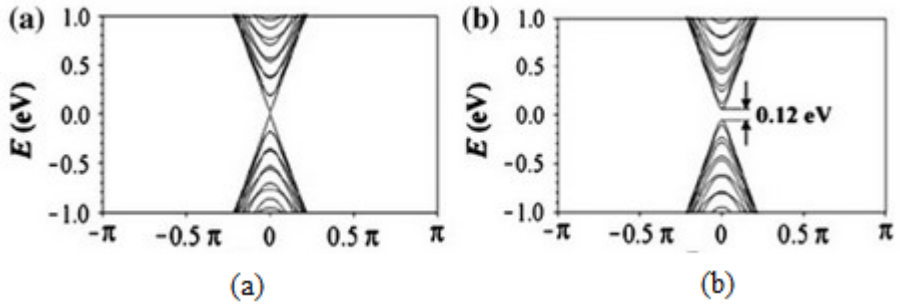

Figure 2.9: (a) Metallic ac-GNR (b) Semiconducting ac-GNR [25].

GNRs can be classified as single-layer GNR (SLGNR) and multi-layer GNR (MLGNR) depending on the number of graphene sheets used. In SLGNR, single graphene layer is present whereas in MLGNR, multiple layers of graphene sheet

are present. These are shown in Figures 2.10(a) and 2.10(b) respectively [1]. MLGNR is mostly preferable over SLGNR, due to lower resistivity. In case of MLGNR, dopped MLGNRs are also used for improvement in conductivity [26].

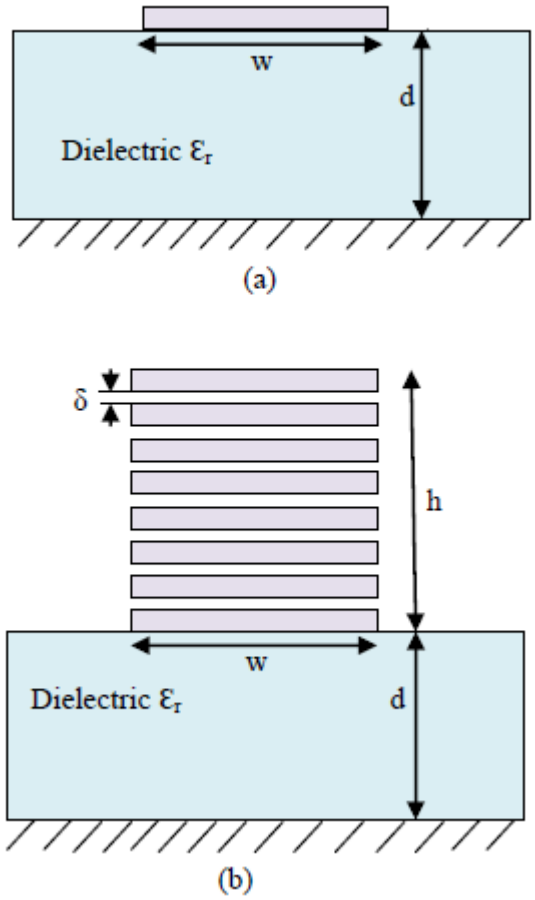

Figure 2.10: Schematic of (a) SLGNR (b) MLGNR interconnect.

MLGNR can also be classified as top contact (TC-MLGNR) and side contact (SC-MLGNR) as shown in Figure 2.11. SC-MLGNR is better over top contact. This is due to better contact between all the layers in the side contact configuration. This leads to lower contact resistance [27].

Various researches have been performed in CNT and GNR interconnects. A simple circuit model for metallic SWCNT using the Luttinger liquid theory with spin charge was presented in [28-29]. The author has predicted impedance with respect to frequency. Distributive electrical circuit model formulation for SWCNT was proposed in [30-32]. Similarly, circuit model for MWCNT has been presented in [33]. Modeling of bundle interconnects using ESC model and its Nyquist stability analysis have been proposed in [21, 34].

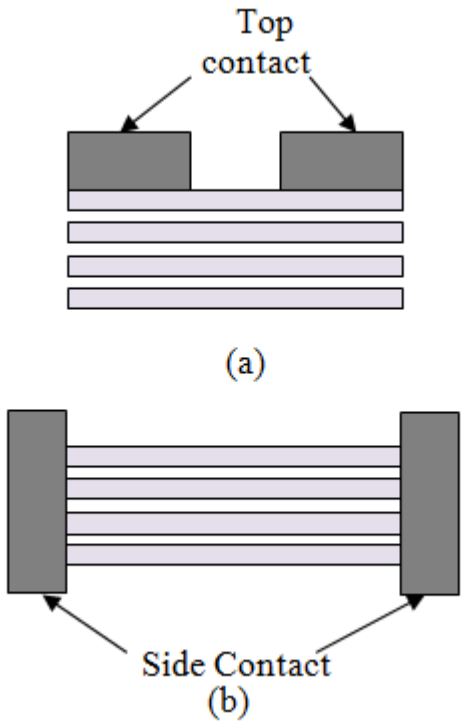

Figure 2.11: (a) Top contact MLGNR (b) side contact MLGNR interconnects.

Circuit models of monolayer and multilayer GNR have been proposed in [35, 36] which is another important structure of graphene. Naeemi *et al.* have described physics-based equivalent circuit models with armchair and zigzag graphene nanoribbons (GNRs), evaluated performance of their conductance and benchmarked against carbon nanotubes and copper wires [35]. Mechanical properties of suspended graphene sheets have been detailed in [36]. Atul *et al.* have performed on analytical time domain model for GNR interconnects with SC-MLGNR and TC-MLGNR configuration. They have validated their analytical model results with SPICE model [27]. The authors have also given the self consistent capacitance model for multilayer graphene nanoribbon interconnects in [37]. Time and frequency domain analysis have been conducted on MLGNR and CNT interconnects using ABCD parameter model in [22, 38, 39]. Numerical method based FDTD model formulation for the analysis of CNT and GNR interconnects have been presented in [40-42].

2.3 Subthreshold region of operation

In subthreshold region, ideally there is no current flow between source and drain of MOSFET. However, due to parasitics and non-ideal effects, some leakage current flows through the MOSFET [3]. During subthreshold region of operation gate voltage (V_{gs}) is lower or equivalent to threshold voltage (V_{th}) of MOSFET i.e. $V_{gs} \leq V_{th}$ [9]. The current in subthreshold region varies exponentially with V_{gs} and is given as:

$$I_D = \frac{\mu_n C_{OX} W}{L}(\eta - 1)V_T^2 e^{\frac{V_{gs}-V_{th}}{\eta V_T}} \left(1 - e^{-V_{ds}/V_T}\right) \tag{2.7}$$

where, V_{ds} is the drain to source voltage, W and L are respectively width and length of MOSFET, C_{OX} is the oxide capacitance , V_T is thermal voltage and η is slope factor and is defined as:

$$\eta = 1 + \frac{C_D}{C_{OX}} \tag{2.8}$$

where, C_D is depletion layer capacitance.
Subthreshold region of operation is one of the most efficient techniques to attain low power in circuits and systems. For ultra low power applications, performance analysis of interconnect in subthreshold region has been performed by many researchers. Analytical modeling of copper interconnect in subthreshold region of operation has been formulated in [43-44]. In [43] various crosstalk effects in copper interconnect operating at subthreshold region is analyzed. To attain high performance, repeater insertion method along with subthreshold region has been investigated in [44].

CHAPTER 3
Performance Improvement Techniques in On-chip Interconnects

There are hand full of techniques by which the performance of on-chip interconnects can be escalated. Some of these are discussed here as follows:

3.1 Wire engineering

Wire engineering is an effective method in which both delay and cross talk can be reduced. In wire engineering technique, dimensions of wire are optimized to attain high performance. Wire engineering includes wire sizing, wire spacing and wire ordering.

3.1.1 Wire sizing

Wire sizing is the technique of modulating wire width. Starting from the driver point, the size of the wire reduces towards the receiver point. The sizing of the wire can be uniform or non-uniform. These are shown in Figure 3.1(a) and (b). The exact wire sizing dimensions are derived by applying optimization schemes so as to improve the performance of the wire. The wire width reduction towards the receiver side decreases capacitance while there is increase in resistance of the wire. However, owing to small charge in-out flow at the receiver side, the impact of increase in resistance due to wire tapering is nominal [45].

3.1.2 Wire spacing and ordering

Wire spacing is for proper optimizing space that is left after routing. Optimizing tree network of interconnect structure is done in a way that it will not change its topology. Wire ordering is the method of reordering of wire for delay and power optimization. Reordering of wire is based on the driver strength.

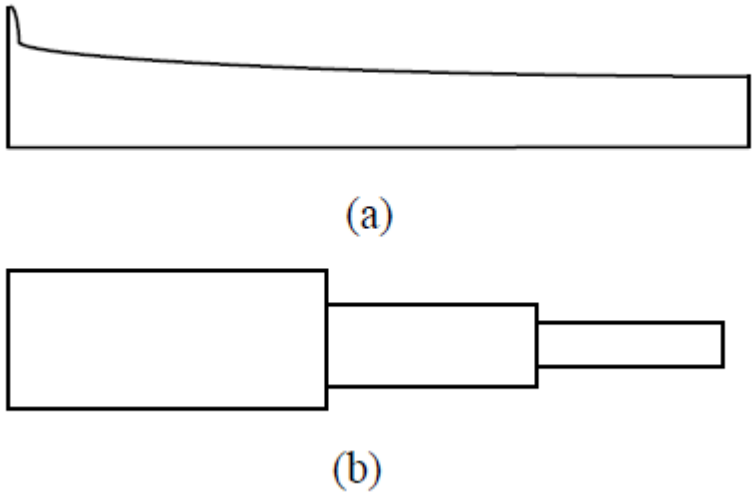

Figure 3.1: Wire sizing (a) uniform (b) non-uniform.

3.2 Shielding

As technology advances, devices and interconnects are more compactly packed in an IC. As a result, chip density increases. Shielding is an effective technique for reduction of crosstalk and delay uncertainties. The basic idea of shielding is to reduce capacitive and inductive coupling effects by providing shield in between the elements where such effects occurs. This is shown in Figure 3.2. Shielding removes undesirable coupling effects. However, shielding has some disadvantages like it consumes more power, increases routing area and add on complexity [46].

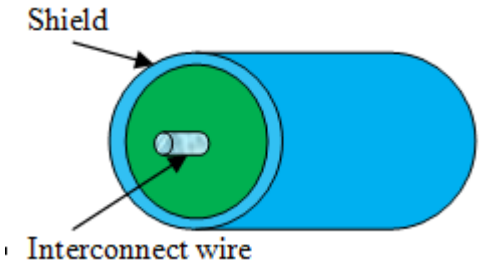

Figure 3.2: Schematic of shielded wire.

3.3 Repeater insertion

At deep sub micron (DSM) technologies, interconnect delays are more than gate delays which is not desirable. This needs to be reduced [45]. Various techniques

have been proposed to improve the performance of interconnects [46]. Repeater insertion is one of the effective methods that has been suggested by many researchers [47, 48]. In repeater insertion method, buffers are inserted in long interconnects. This reduces the length of wire that effectively decreases latency in the circuit. However, there are some practical limitations of the repeater insertion method. Repeaters have to be properly sized and should be fixed at proper intervals to achieve optimum outputs [49-50].

3.4 Method of signaling

Method of signaling is another efficient performance improvement technique. Signaling scheme defines the signal levels over interconnects. Broadly two types of on-chip signaling schemes are there. One is voltage mode signaling and the other is current mode signaling. In current mode signaling, voltage level over interconnect is reduced. This causes fast charging and discharging of interconnect parasitic node capacitances. As a result delay in current mode signaling scheme reduces. To improve the performance of interconnects, current mode signaling has been proposed in [42, 51-54]. It is shown that current mode system has lesser delay and higher throughput than voltage mode system.

3.5 Interconnect material

Many materials are employed in interconnects, in which copper is the most widely used material. The resistivity of Cu interconnects increases rapidly because of the effects of enhanced grain surface scattering, longer interconnect length, higher operating frequency and Joule heating. Increased heating and high temperature further stimulates electro-migration induced hillocks and voids formation. These cumulatively limit the performance and cause signal integrity, skin effect, higher power dissipation and crosstalk in ICs [2], [4]. Figure 3.3 shows the effect of scaling of copper, aluminum, siliside and tungsten interconnects with the feature size. It determines the impact of scaling on different feature size of interconnects. It also facilitates in determining the longest interconnection length for the best performance of a given material at given technology node[55].

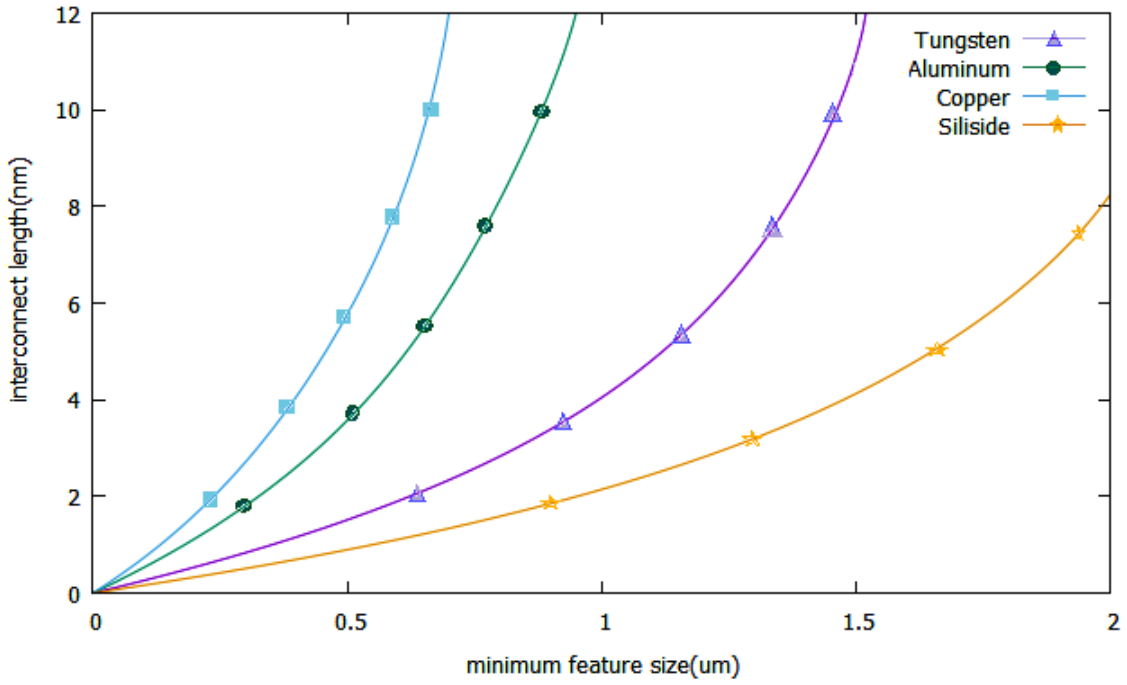

Figure 3.3: Effect of scaling on interconnections materials.

From the analysis, it is evident that at nano-dimensions copper have limited significance. In pursuit to attain higher and sustainable performance at nanometer technologies, several researches have been made. Graphene derived New material CNTs and GNRs have been investigated as a new material in on-chip interconnect applications [35].

CHAPTER 4
Mathematical Modeling Techniques for Interconnect System

Several mathematical models have been proposed for the performance analysis of interconnects. A few of the prominent techniques enumerated here are moment matching, two-port modeling and numerical method based finite-difference time-domain (FDTD).

4.1 Moment matching technique

Moment matching technique is the method of estimating dominant system parameters. Moments define the circuit characteristics such as delay and power dissipation [56]. For defining moment, Taylor's series is used to expand the transfer function $H(s)$ at point $s = 0$,

$$H(s) = H(0) + s\frac{H(0)^{(1)}}{1!} + s^2\frac{H(0)^{(2)}}{2!} + \cdots + s^n\frac{H(0)^{(n)}}{n!} \tag{4.1}$$

where, the superscript n denotes the n^{th} derivative. This can be equivalently denoted as,

$$\begin{aligned} H(s) &= m_0 + m_1 s + m_2 s^2 + \cdots + m_n s^n \\ &= \sum_{i=0}^{n} m_i s^i \end{aligned} \tag{4.2}$$

where, $m_i = \frac{H(0)^i}{i!}$. The coefficients of Taylor's series expansion m_i are called moments [56].

4.1.1 Elmore model

A system with first order moment approximation is known as Elmore model. Elmore model is a simple technique to calculate delay of *RC* network in any electronic system. Owing to its simplistic nature of modeling and ability to produce considerable accurate results, this model is used in variety of applications as logic synthesis, static timing analysis, placement and routing. For arbitrary *RC* network, delay of any path can be computed by R times the C of the given path. This is equivalent to moment matching technique with one moment [57]. Elmore model can be extended and improved by considering upper bounds and lower bounds for obtaining more accurate results [58-59].

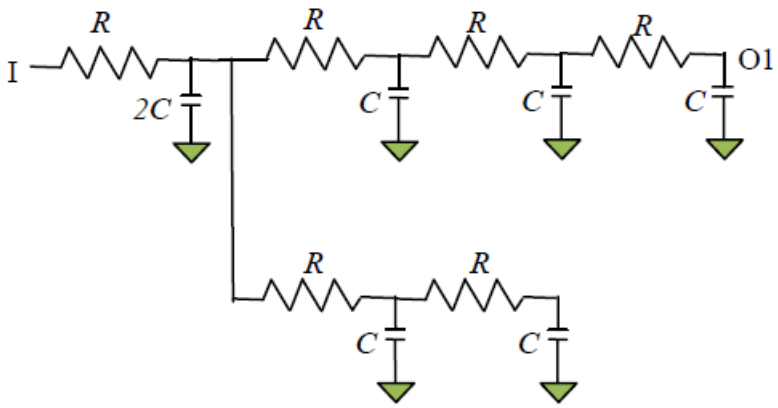

Figure 4.1: RC tree structure.

The delay of RC circuit (show in Figure 4.1) using Elmore delay can be computed as:

$$T_{di} = \sum_{k=1}^{N} R_{ki} C_k \tag{4.3}$$

where R_{ki} is the total resistance of the path between the input node and i^{th} node and it has to be common with the path between the input and node k, C_k is the capacitance at node k [58]. For example, considering an *RC* network as shown in Figure 4.1, delay T_d between nodes I to O1 using Equation (4.3) is given as:

$$T_d = R.(2C + C + 3C) + 2RC + 3RC + 4RC = 15RC \tag{4.4}$$

The accuracy of the Elmore model can be increased by including more number of moments for computing system performance.

4.1.2 Higher order moment matching

Consideration of higher order moments incorporates the effect of several other system performance governing parameters those were not present while considering the lower order moments. This facilitates in accurately determining the system performance. The transfer function $H(s)$ in Equation (4.1) can be defined as [56].

$$\hat{H}(s) = \frac{b_0 + b_1 s + \cdots + b_L s^L}{1 + a_1 s + \cdots + a_M s^M} \tag{4.5}$$

where, a and b are unknowns (total of $L + M + 1$ variables). Using Taylor's series expansion, Equation (4.5) is modeled as

$$\frac{b_0 + b_1 s + \cdots + b_L s^L}{1 + a_1 s + \cdots + a_M s^M} = m_0 + m_1 s + \cdots + m_{L+M} s^{L+M} \tag{4.6}$$

Using Equation (4.6), the terms with same moments are compared. Owing to moment matching, this method is called as moment matching technique. By comparing the moments, all the coefficient values can be obtained. These are derived as,

$$\begin{aligned} a_0 &= m_0 \\ a_1 &= m_1 + b_1 m_0 \\ &\vdots \\ a_L &= m_L + \sum_{i=1}^{min(L,M)} b_i m_{L-i} \end{aligned} \tag{4.7}$$

4.2 Two-port network

A two-port network has four terminals (two at the input side and the other two at the output side). This comprises of different network topologies for modeling electric circuits. The generalized model is shown in Figure 4.2 [60-61]. In a two-port network, generally port 1 is considered as the input port and port 2 is considered as the output port.

Some of the widely used two ports topologies are z, y, h, g and ABCD. For example, detailing one of the widely used two port model viz. ABCD as:

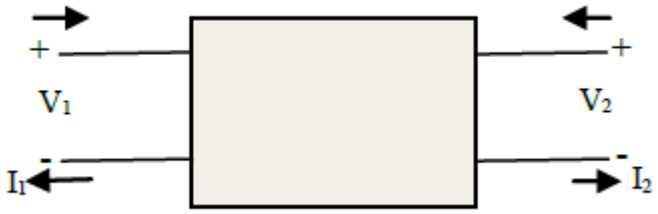

Figure 4.2: Two port network model.

4.2.1 ABCD model

The ABCD model is widely used for on-chip interconnect modeling and analysis [25, 38]. In ABCD model, each interconnects line is modeled using ABCD matrix. From the two-port ABCD model theory, voltage and current of an ABCD model are derived as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{4.8}$$

where, $A = \frac{V_1}{V_2}$, $B = -\frac{V_1}{I_2}$, $C = \frac{I_1}{V_2}$, $D = -\frac{I_1}{I_2}$

The ABCD-parameters are also known as transmission parameters.

For modeling and analysis using ABCD model, on-chip interconnect is replaced by equivalent ABCD matrix. For arbitrary interconnect structure, the main path along with each of its branches are represented by ABCD matrices. The subtrees of the main module are marked by respective admittances. This is shown in Figure 4.3(a). V_1 and V_{N+1} represent voltages at source and sink. The ladder network in Figure 4.3(a) is solved to formulate equivalent ABCD model. This is shown in Figure 4.3(b). The equivalent ABCD model for the ladder network is indicated by $[ABCD]_n$.

The transfer function for the module between node n and $n+1$ in Figure 4.3(a) can be derived as

$$H_n(s) = \frac{1}{A + BY_{n,L}} \tag{4.9}$$

where, $Y_{n,L}$ is the load admittance of sub-path. To compute $Y_{n,L}$, input admittance of the post-order network is required. Consequently $Y_{n,in}$ is computed as,

$$Y_{n,in} = \frac{C + DY_{n,L}}{A + BY_{n,L}} \tag{4.10}$$

The transfer function of the equivalent network in Figure 4.3(b) is obtained as:

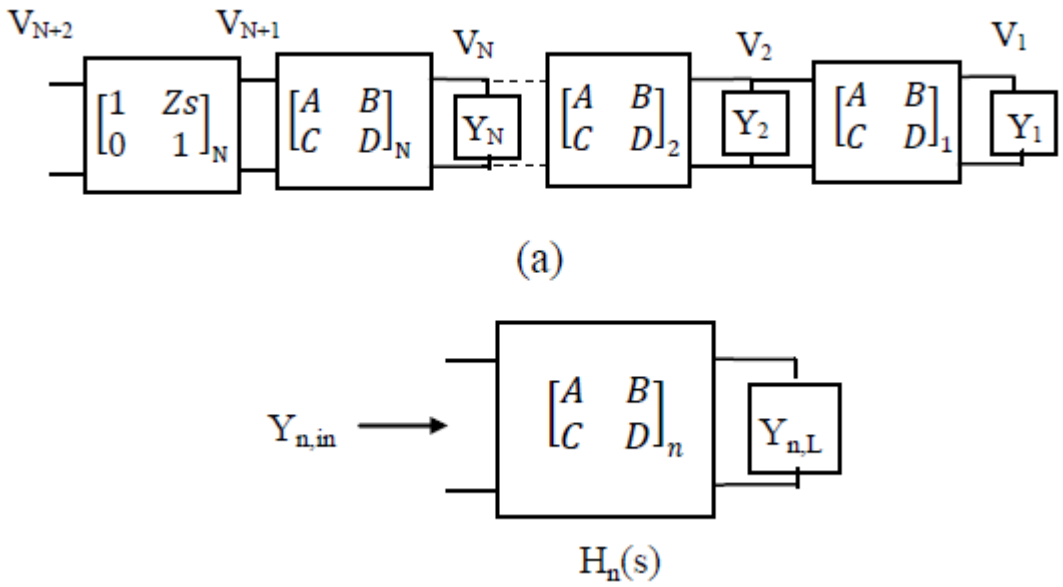

Figure 4.3: On-chip interconnect modeling using ABCD model.

$$H(s) = H_s(s)H_n(s)H_{n-1}(s)\dots H_1(s) \tag{4.11}$$

where, $H_n(s)$ is the transfer function between the node n and n+1. $H_s(s)$ is the transform function between the source and the node $n+1$ [38-62].

4.3 Numerical method analysis

Broadly interconnect analysis algorithms can be classified into two methods as: (1) circuit method and (2) electromagnetism method [40]. In circuit-based method analysis, interconnect is approximated as lumped or distributed parameters. This is already discussed in the previous section. In electromagnetism method, interconnects can be equivalently represented as 2D or 3D models. These are then solved using Maxwell equations and Full wave method. The accuracy of electromagnetism method is higher. However, it is computationally expensive [40]. A few techniques based on electromagnetic numerical method are finite element method (FEM) and finite difference time domain (FDTD) method [40]. These are briefly discussed here as follows:

4.3.1 Finite element method

Finite element method is used for solving problems of engineering and mathematical physics. This method involves application of boundary conditions to

solve the partial differential equations. In this method, large segment of considered part is divided into small segments that are called finite elements. Typically this method is employed for variety of applications such as structural analysis, fluid flow, heat transfer, mass transport, and electromagnetic potential [63].

4.3.2 Finite-difference time-domain (FDTD) method

The interconnect system comprises of driver, interconnect and load (DIL) subsystems. Conventionally, modeling of driver and load were performed in time domain while interconnect were modeled in frequency domain. These cause time - frequency or reverse conversion problem [40]. To mitigate this issue, FDTD model has been found appropriate. It gives accurate results and takes less CPU time for computation [31]. FDTD technique was firstly introduced by Kane Yee in 1966 [64]. He found the discrete solution of the Maxwells curl equations by use of central difference approximations. The FDTD method discretizes the Maxwells curl equations and simulates it [40, 64]. Many researchers have used FDTD technique as mathematical model to analyzes DIL system [40, 48,64]. The DIL system is presented in Figure 4.4. The driver is CMOS inverter. The interconnect is modeled by distributed *RLC* segments. This is shown in Figure 4.5. Δx represents the small distance. The receiver(load) is equivalently modeled as capacitance. In FDTD method, voltage and current variables are computed in time and space domains alternatively. This is shown in Figure 4.6. In FDTD method, the interconnect line is divided into N divisions. In FDTD method, the interconnect line is divided into N divisions. The first step in implementing FDTD method is to define number of points in space and time domains. Total points along space and time are K and N respectively. Along space and time domains, points are discretized as $k\Delta x$ and $n\Delta t$ respectively, where k and n are integer and defined as$1 \leq k \leq K$ and $1 \leq n \leq N$ [40].

The voltage and current along interconnect can be defined by Telegrapher's equations as:

$$\frac{\partial v(x,t)}{\partial x} = -\left\{ Ri(x,t) + L\frac{\partial i(x,t)}{\partial t} \right\} \tag{4.12}$$

$$\frac{\partial i(x,t)}{\partial x} = -\left\{ C\frac{\partial v(x,t)}{\partial t} \right\} \tag{4.13}$$

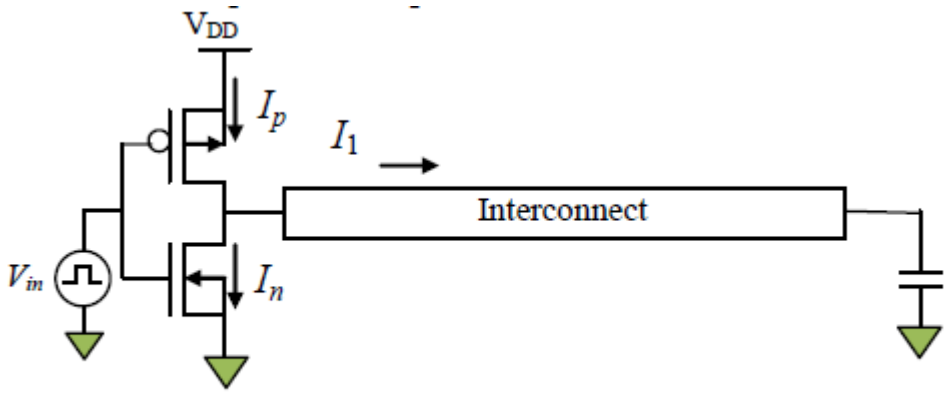

Figure 4.4: Driver-interconnect-load (DIL) model.

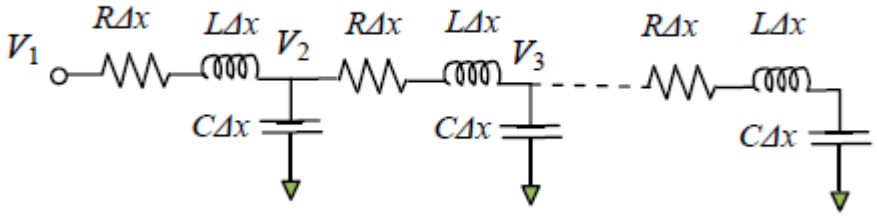

Figure 4.5: Distributed transmission line model.

By applying central difference approximation, we get

$$\frac{(v_{k+1}^n - v_{k-1}^n)}{2\Delta x} = -\left(Ri_k^n + L\frac{(i_k^{n+1} - i_k^{n-1})}{2\Delta t}\right) \tag{4.14}$$

$$\frac{(i_{k+1}^n - i_{k-1}^n)}{2\Delta x} = -\left(C\frac{(v_k^{n+1} - v_k^{n-1})}{2\Delta t}\right) \tag{4.15}$$

Using these equations, voltage and current at any particular node in space and time can be derived as:

$$i_k^{n+3/2} = BDi_k^{n+1/2} + B(v_k^{n+1} - v_{k+1}^{n+1}) \tag{4.16}$$

where,

$$B = \left[\frac{\Delta x}{\Delta t}L + \frac{\Delta x}{2}R\right]^{-1},\ D = \left[\frac{\Delta x}{\Delta t}L - \frac{\Delta x}{2}R\right]$$

$$v_k^{n+1} = v_k^n + A(i_{k-1}^{n+1/2} - i_k^{n+1/2}) \tag{4.17}$$

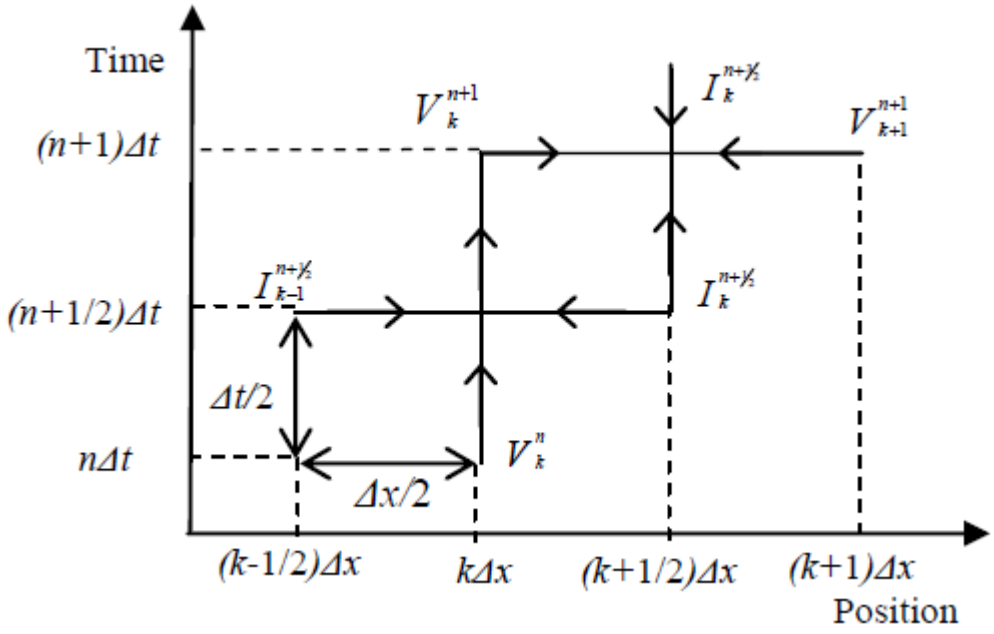

Figure 4.6: Discretization of voltage and current along space and time.

where,

$$A = \left[\frac{\Delta x}{\Delta t}C\right]^{-1}$$

Using these equations, voltage and current are computed along interconnect. To define the deriving source at the driver-end and load at far receiver-end, near-end and far-end boundary conditions respectively need to be expressed. These are described as follows:

4.3.3 Near-end boundary condition

Using equation (4.17) and keeping k equal to 1 for near-end boundary condition results:

$$V_1^{n+1} = V_1^n + 2A\left[\frac{I_0^{n+1} + I_0^n}{2} - I_0^{n+1/2}\right] \tag{4.18}$$

Initial current can be calculated by applying KCL at near-end boundary node i.e. V_1.

$$I_0 = C_m\left[\frac{d(v_s - v_1)}{dt}\right] + I_p - I_n - c_d\frac{dv_1}{dt} \tag{4.19}$$

I_n and I_p formulations are shown in equations (4.20), (4.21), (4.22) and (4.23) respectively. I_n and I_p are derived using equation (2.7). For large V_{ds}, i.e. $V_{ds} \leq 4V_T$, term in (2.7) approaches unity. These are defined by equation (4.20) and (4.22). For smaller value of V_{ds}, that term has considerable value and its value is obtained by

expanding the term using Taylor's series. Depending on V_{ds} value, current I_n and I_p are divided into two region as shown below [3]:

$$I_n = \frac{\mu_n C_{OX} W}{L}(n-1)V_T^2 e^{\frac{V_{gs}-V_{th}}{nV_T}}, \text{ if } V_{ds} \geq 4V_T \tag{4.20}$$

$$I_n = \frac{\mu_n C_{OX} W}{L}(n-1)V_T V_{ds}, \text{ if } V_{ds} < V_T \tag{4.21}$$

$$I_p = \frac{\mu_n C_{OX} W}{L}(n-1)V_T^2 e^{\frac{V_{gs}-V_{th}}{nV_T}}, \text{ if } V_{ds} \geq 4V_T \tag{4.22}$$

$$I_p = \frac{\mu_n C_{OX} W}{L}(n-1)V_T V_{ds}, \text{ if } V_{ds} \leq V_T \tag{4.23}$$

4.3.4 Far-end boundary condition

At far-end i.e. at receiver, voltage is defined by substituting $k = Nx + 1$ in equation (4.17).

$$V_{Nx+1}^{n+1} = V_{Nx+1}^{n} + 2A\left[I_{Nx}^{n+1/2} - \frac{I_{Nx+1}^{n+1} + I_{Nx+1}^{n}}{2}\right] \tag{4.24}$$

Due to capacitive load, output current is obtained as:

$$I_{Nx+1} = C_L \frac{d}{dt} V_{Nx+1} \tag{4.25}$$

By discretizing and placing it in equation (4.24) far-end voltage can be given as:

$$V_{Nx+1}^{n+1} = V_{Nx+1}^{n} + 2FA\left[I_{Nx}^{n+1/2} - \frac{I_{Nx+1}^{n}}{2}\right] \tag{4.26}$$

$$F = \left[U + \frac{AC_L}{\Delta t}\right]^{-1} \tag{4.27}$$

CHAPTER 5
Interconnect Modeling for Electrical Equivalent Parameters Extraction

In this section *RLC* wire parasitics associated with copper and graphene interconnects are derived.

5.1 Electrical modeling parameters of copper interconnect

The schematic of copper over ground plane is given in Figure 5.1, where h represents height of copper from ground plane and t is the thickness of copper. Equivalent circuit model of copper interconnect is shown in Figure 5.2.

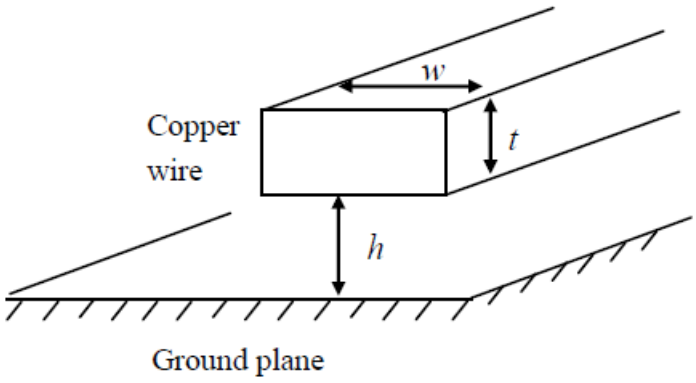

Figure 5.1: Copper wire over ground plane.

The formulations of parasitic elements of copper are detailed below [65]. The resistance of copper wire is given as:

$$R_{cu} = \frac{\rho l}{A} = \frac{\rho l}{t.w} \tag{5.1}$$

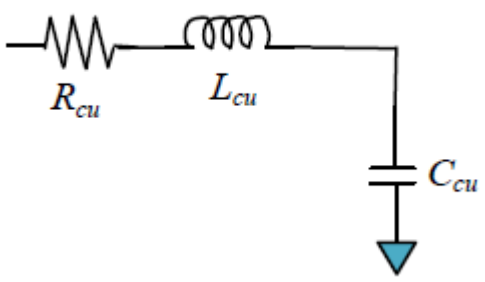

Figure 5.2: Equivalent circuit model of Cu interconnect.

where, ρ is the resistivity of material, l is the length of wire, A is the area of wire and w is the width of wire.

The capacitance of copper wire is given as:

$$C_{cu} = \epsilon \left[\left(\frac{w}{h} \right) + 2.04 \left(\frac{s}{s + 0.54h} \right)^{1.77} \left(\frac{t}{t + 4.53h} \right)^{0.07} \right] \tag{5.2}$$

where, ϵ is the dielectric permittivity and s is the inter-wire spacing. The inductance of copper wire is given as:

$$L_{cu} = 2 \times 10^{-7} l \left(\log \left(\frac{2l}{w + h} + 0.5 + \frac{w + h}{3l} \right) \right) \tag{5.3}$$

5.2 Electrical modeling parameters of CNT interconnect

The schematic of CNT over ground plane is given in Figure 5.3 in which h represents height of CNT from ground plane and d is the diameter of CNT. The circuit model of SWCNT interconnect is shown in Figure 5.4. The resistances of SWCNT comprises of three components: quantum resistance (R_Q), imperfect contact resistance (R_{mc}) and scattering-induced ohmic resistance (R_O) [66]. R_Q is given as

$$R_Q = \frac{\hbar}{4e^2} \tag{5.4}$$

where $\hbar$ is Planck's constant and equal to $6.626 \times 10^{-34} J.s$, and e is the electronic charge $(= 1.6 \times 10^{-19} C)$ [67]. R_{mc} ranges from zero to a few kilo ohms depending on different fabrication processes. R_Q and R_{mc} together constitute lumped resistance of SWCNT (R_{lump}). R_o of SWCNT is given by,

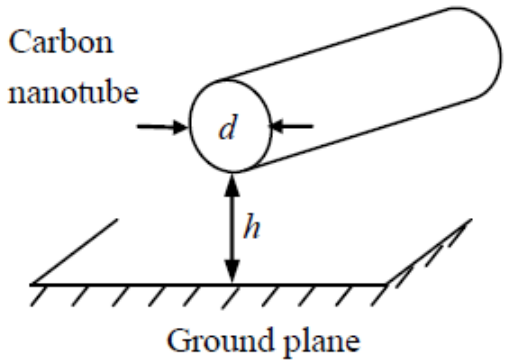

Figure 5.3: Single wall carbon nanotube (SWCNT) over a ground plane.

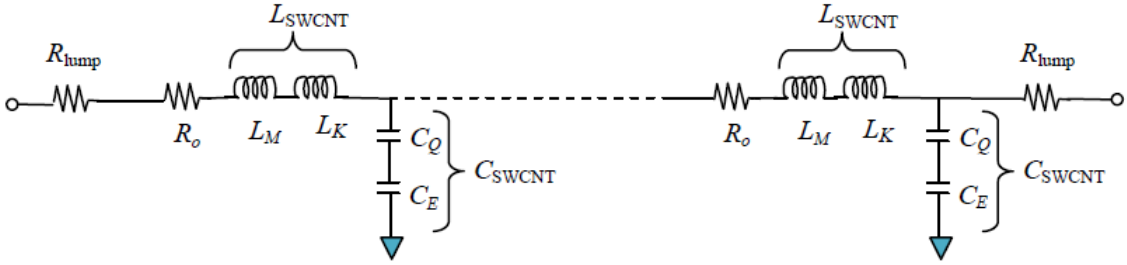

Figure 5.4: Equivalent circuit model of CNT.

$$R_0 = \frac{R_Q}{\lambda} \tag{5.5}$$

where, λ is the mean free path length [68]. Magnetic inductance of SWCNT is given by

$$L_M = \frac{\mu}{\pi} ln\left(\frac{h}{d}\right) \tag{5.6}$$

where, μ is dielectric permeability. The kinetic inductance is given as:

$$L_K = \frac{\hbar}{2e^2 v_F} \tag{5.7}$$

where, v_F is Fermi velocity. The SWCNT capacitance comprises of two parts. One is called electrostatic capacitance (C_E) and the other one is called quantum capacitance (C_Q). The electrostatic capacitance is evaluated as:

$$C_E = \frac{2\pi\epsilon}{ln(h/d)} \tag{5.8}$$

For $h = 1\mu m$ and $d = 1nm$, electrostatic capacitance is calculated numerically

using Equation (5.8) and is $C_E = 50aF/\mu m$. The quantum capacitance is given as:

$$C_Q = \frac{2e^2}{hv_F} \tag{5.9}$$

The total inductance and capacitance of SWCNT is given by,

$$L_{SWCNT} = L_M + L_K;\ C_{SWCNT} = \frac{C_E C_Q}{(C_E + C_Q)} \tag{5.10}$$

5.3 Electrical modeling parameters of GNR interconnect

Mono-layer GNR has very high resistance, hence multilayer GNR (MLGNR) structure is often used for VLSI interconnects. This is shown in Figure 5.5 [66].

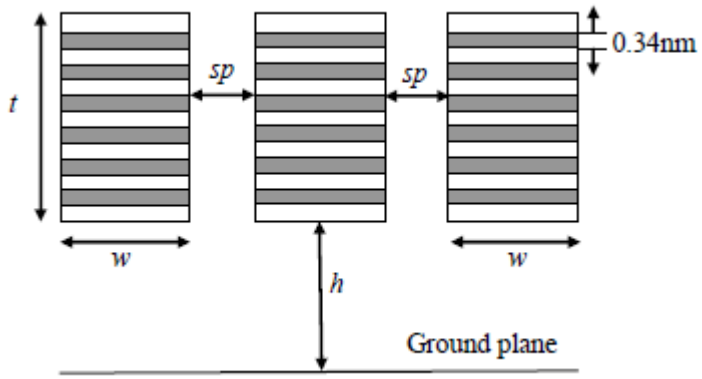

Figure 5.5: Schematic of multilayer GNR interconnect.

The thickness and width of the GNR are denoted by t and w, respectively. Interconnect height from the ground plane is h, and sp is the spacing between two interconnects. The separation between each graphene layer is known as Vander Waals gap which is equal to $\delta(= 0.34nm)$ [69]. The number of graphene layer in MLGNR is given as:

$$N_{layer} = (1 + Integer(t/\delta)) \tag{5.11}$$

Figure 5.6 shows the equivalent circuit diagram of a *RLC* model of multi-layer GNR where R_o, L_{GNR} and C_{GNR} represent the distributed resistance, inductance and capacitance of GNR interconnect. L_{GNR} comprises of kinetic inductance (L_K)

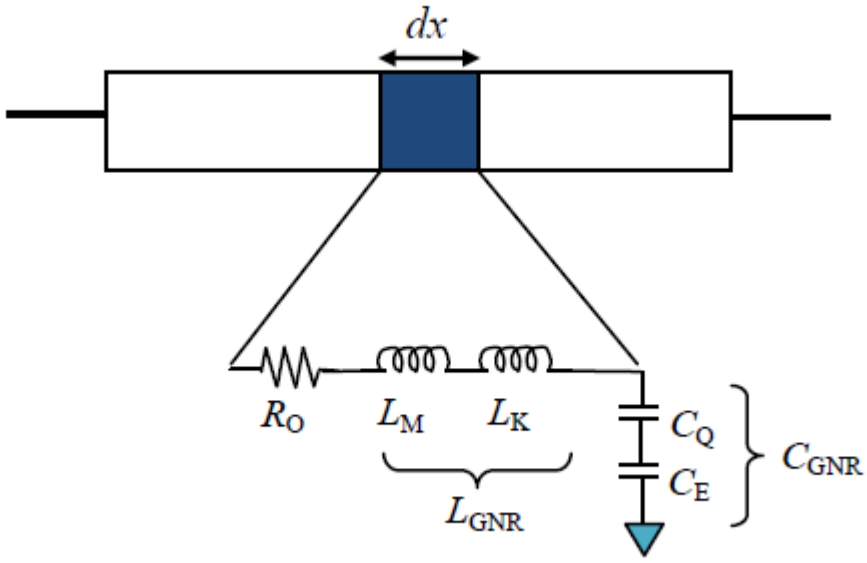

Figure 5.6: Equivalent circuit model of monolayer GNR.

and magnetic inductance (L_M). C_{GNR} comprises of electrostatic capacitance (C_E) and quantum capacitance (C_Q) [70].
The resistance of monolayer GNR is expressed as:

$$R_{GNR} = \frac{\hbar/2e^2}{N_{ch}N_{layer}} \tag{5.12}$$

where N_{ch} is the number of conducting channels (modes) in one layer, N_{layer} is the number of GNR layers, C_Q and C_E are the quantum and electrostatic capacitance respectively. The per unit length quantum capacitance C_Q and electrostatic capacitance C_E are expressed as [67]:

$$C_E = \frac{\epsilon w}{d} \tag{5.13}$$

$$C_Q = N_{ch}N_{layer}\frac{4e^2}{\hbar v_F} \tag{5.14}$$

The per unit length kinetic inductance (L_K) and magnetic inductance (L_M) are expressed as [69],

$$L_M = \frac{\mu d}{w} \tag{5.15}$$

$$L_k = \frac{(\hbar/4e^2)v_F}{N_{ch}N_{layer}} \tag{5.16}$$

Total inductance and capacitance of GNR is given as,

$$L_{GNR} = L_M + L_K,\ C_{GNR} = \frac{C_E C_Q}{C_E + C_Q} \tag{5.17}$$

CHAPTER 6
Results and Discussion

In this chapter analysis of different interconnect materials in linear and subthreshold regions of operations are presented. The interconnect considered are copper and graphene derived MLGNR interconnect. The performance parameters considered are delay, power and power-delay product.

6.1 Performance analyses of different interconnect materials in linear region

In this section, performance of varying interconnects viz. copper, SWCNT, SWCNT bundle, MWCNT, SLGNR and MLGNR have been analyzed in linear region of operation. The analysis is performed to assess the optimum interconnects at varying length. The driver-interconnect-load (DIL) model is used for the analysis. This is shown in Figure 4.4. V_{in} is the input pulse signal. Delay, power and PDP have been computed for all the interconnect materials. These are shown in Figures 6.1, 6.2 and 6.3 respectively.

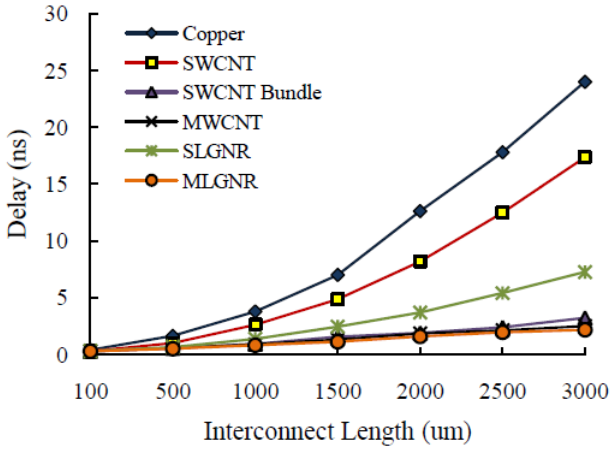

Figure 6.1: Analysis of delay of different interconnect materials with varying interconnect length.

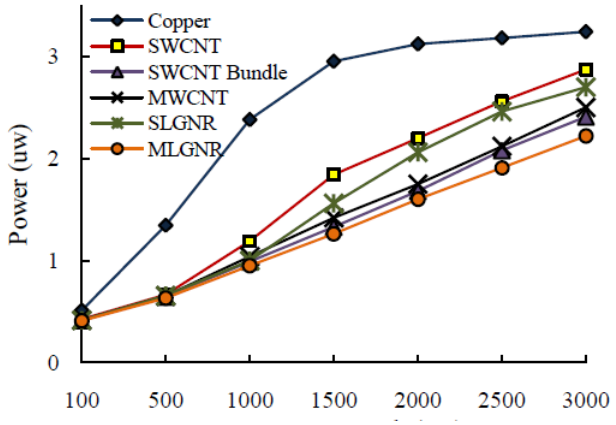

Figure 6.2: Analysis of power of different interconnect materials with varying interconnect length.

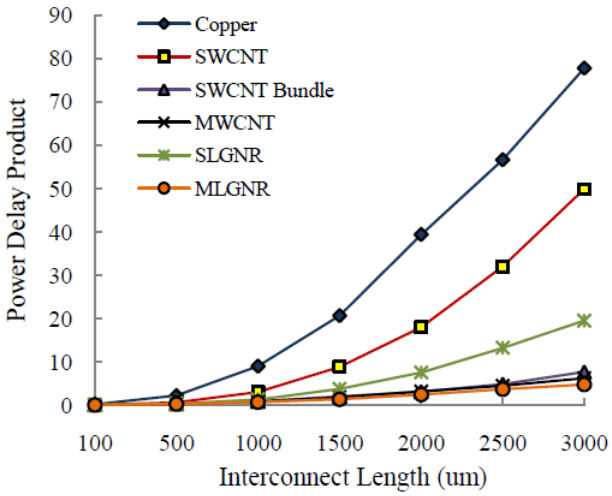

Figure 6.3: Analysis of PDP of varying interconnect materials with varying interconnect length.

Figure 6.1 shows delay variation for different interconnect materials. The interconnect length is varied from 100um to 3000um. It is seen that delay of interconnects increases with wire length. This is due to increase in parasitic impedance of the wire. It is analyzed that MLGNR interconnect has least delay than all other interconnect materials.

Analysis of power of different interconnect materials with varying interconnect length is presented in Figure 6.2. Power increases with interconnect length because of higher wire impedance at longer wire lengths. It is observed that MLGNR has least power dissipation than other interconnects.

Figure 6.3 shows the variation in power-delay product (PDP) with interconnect

length. PDP is the figure of merit of system which indicates overall performance efficiency of the system. Lower PDP signifies better performance. From the figure it is seen that MLGNR interconnects possess smaller PDP. This signifies the superior performance of MLGNR interconnects over all other interconnects.

6.2 Performance analyses of different interconnect material using proposed FDTD model in subthreshold region of operation

The technology node used is 22nm for the performance analysis of different interconnects materials. Width and spacing of interconnect is 22nm. Thickness and height of interconnect are taken as 44nm [71].

6.2.1 Transient analysis

The driver-interconnect-load (DIL) model is used for the analysis. V_{in} is the input pulse signal with signal transition time of 10ns and pulse period of 1us. For the linear and subthreshold regions of operation analysis, input voltages considered are 0.9V and 0.3V respectively. Transient output of both regions for copper and graphene are shown in Figure 6.4. It is seen that the voltage swing in subthreshold region is reduced as compared to linear region. The smaller swing in subthreshold region is because of smaller voltage supplied at the input terminal. In Figure 6.4, SPICE simulation results are compared with proposed FDTD based model. It is analyzed that the average percentage error between the proposed mathematical and simulation models in case of linear region is 0.18%. This value for subthreshold region of operation is 0.26%. Hence proposed FDTD based model matches very closely with the SPICE simulation results.

6.2.2 Delay, power and PDP analyses with varying interconnect length

Using the DIL model delay, power dissipation and power-delay product (PDP) have been computed for copper and MLGNR interconnects. In Figures 6.5-6.7 delay, power dissipation and PDP are computed with respect to varying interconnect length. Figure 6.5 shows delay variation of copper and MLGNR interconnect in subthreshold and linear regions. The interconnect length is varied from 100um

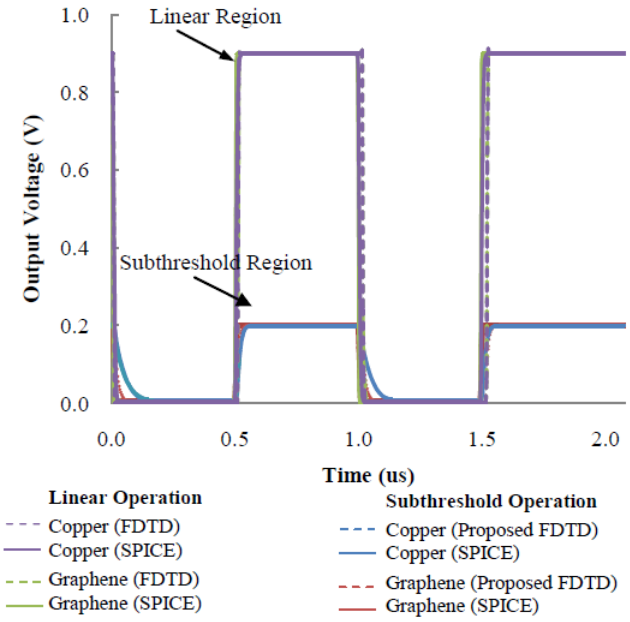

Figure 6.4: Transient analysis of copper and graphene interconnect at linear and subthreshold regions of operation.

to 3000um. Delay of interconnects increases with respect to wire length due to increased impedance of the wire at longer length. It is analyzed that MLGNR interconnect has least delay than copper interconnect. In subthreshold region, delay is comparatively higher as compared to linear region. This is because, circuit performance becomes slow in subthreshold region. For example, at 1000um interconnect length, delay is about 4.9 times higher in subthreshold region as compared to linear region for copper interconnect whereas for graphene interconnects, delay in subthreshold region is 4.6 times higher than its counterpart linear region.

Analysis of power dissipation in copper and MLGNR interconnects with varying interconnect length can be studied from Figure 6.6. It is seen that in subthreshold region, power consumption is lower than linear region. For example, at 1000um interconnect length, power dissipation in subthreshold region is about 9 and 12 times lower than linear region for copper and MLGNR interconnect respectively. The lower power dissipation in subthreshold region of operation allows its usage effectively in ultra low power applications. It is also analyzed that MLGNR interconnect has lesser power dissipation than copper interconnect. Hence MLGNR interconnects together with subthreshold region of operation is prospective high-end solution where low power requirements for circuits and systems are of prime importance.

Figure 6.7 shows the variation in power-delay product (PDP) with interconnect length. PDP is the figure of merit of any system which indicates overall perfor-

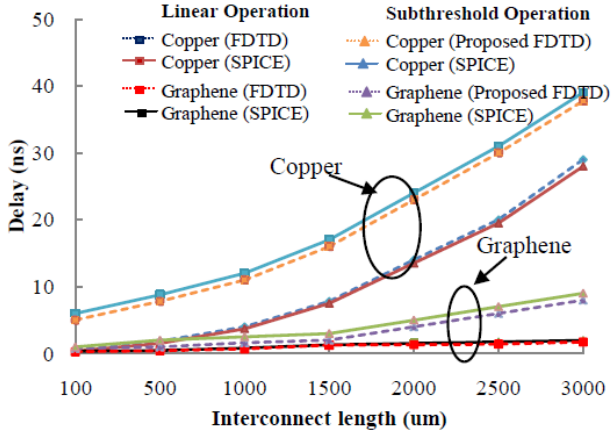

Figure 6.5: Delay analysis of copper and graphene interconnects with varying interconnect length in linear and subthreshold regions of operation.

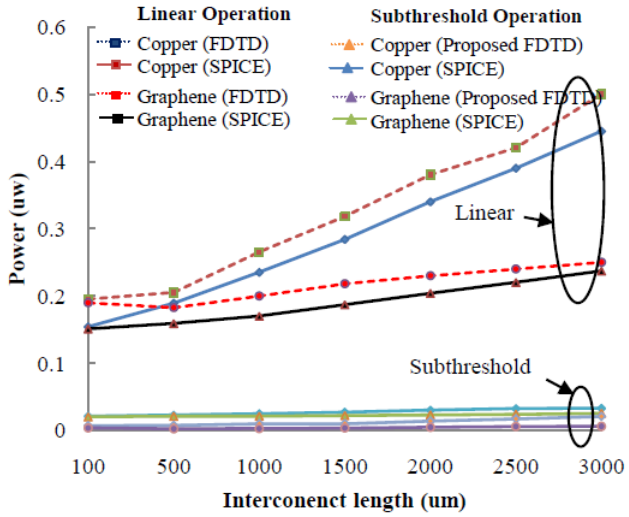

Figure 6.6: Power analysis of copper and graphene interconnects at linear and subthreshold regions of operation with varying interconnect length.

mance efficiency. Lower value of PDP signifies better performance. From Figure 6.7, it seen that MLGNR has lower PDP than copper interconnect hence indicating superior performance. As seen from Figure 6.7, PDP in case of copper and graphene interconnects at 2000um interconnect length in linear region is 5.13fJ and 0.299fJ respectively. Theses values in subthreshold region are 0.3fJ and 0.018fJ. Hence, PDP values in linear and subthreshold regions for graphene interconnect are about 17 and 16 times lower than copper interconnect.

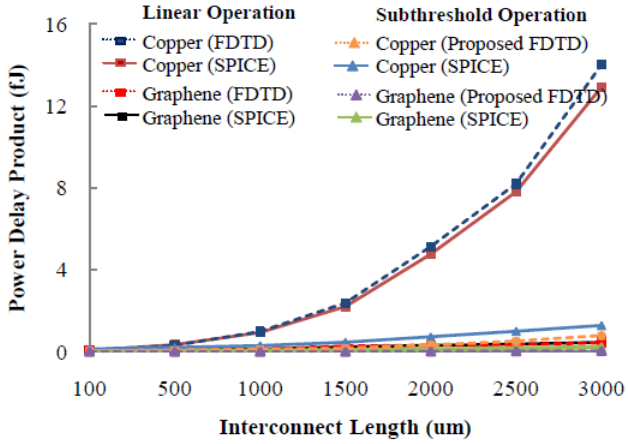

Figure 6.7: PDP analysis of copper and graphene interconnects at linear and subthreshold regions of operation with varying interconnect length.

6.2.3 Delay, power and PDP analyses with varying signal transition period

The performance parameters viz. delay, power dissipation and PDP variation with different signal transition periods are discussed in this section. Signal transition period is varied from 10ns to 100ns. Table 6.1 shows the variation in the all the considered performance parameters with varying signal transition period. The value in bracket '()'shows the percentage variation in the proposed FDTD based model and SPICE results. From the results, it is seen that simulation and proposed mathematical models are in good agreement. In delay analysis, it is seen from Table 6.1 that as expected delay is more in subthreshold region as compared to linear region.

Table 6.1: Performance parameter variation of copper and graphene with varying signal transition period in linear and subthreshold regions of operation.

Signal Transition period (ns)									
Performance Parameter	Interconnect material	10		20		50		100	
		Linear	Sub	Linear	Sub	Linear	Sub	Linear	Sub
Delay (ns)	Copper	3.7 (8)	11 (9)	5 (7.1)	13.8 (8)	7 (8.2)	22 (4)	9.3 (3)	32 (3)
	Graphene	0.2 (8)	4 (6.9)	0.4 (6.8)	7 (8.6)	1.4 (4.3)	9.8 (4.5)	3 (2.1)	13 (3.2)
Power (uw)	Copper	258 (7)	27.2 (8)	355 (8)	27 (8.6)	580 (7)	24 (5)	980 (6)	24 (8)
	Graphene	190 (8)	3 (8)	280 (6)	7 (6.1)	480 (6)	8.7 (5)	850 (4)	10 (6)
PDP (fJ)	Copper	0.9 (0.5)	0.3 (0.5)	1.8 (3.6)	0.4 (2.7)	4 (2.8)	0.5 (8.7)	9.1 (4.1)	0.8 (8.8)
	Graphene	0.03 (1)	0.01(0.5)	0.13 (2)	0.16 (4)	0.7 (6)	0.2 (6)	0.5 (2.5)	0.3 (4)

In case of power dissipation, subthreshold region of operation leads to lower power dissipation. It can be seen that power dissipation ratio of linear to subthreshold interconnects at 10ns, 20ns, 50ns and 100ns are 9, 12, 13 and 19 respectively for copper interconnects. These power dissipation ratios in case of graphene interconnects are 8, 11, 9 and 14 respectively. The higher than unity value of power dissipation ratio values in both copper and graphene interconnects indicate that the subthreshold region of operation possesses lower power dissipation hence good for lower power applications. The figure of merit is also computed and shown in Table 6.1. For all cases considered, it is seen that PDP is lower in case of subthreshold region of operation. Hence, graphene and subthreshold region of operation stand good for different interconnect lengths and varying signal transition periods.

CHAPTER 7
Variability Analysis

The term variability refers to the fluctuation in parameters under consideration. At nano-dimensions, variation due to process, voltage and temperature results in fluctuation of output system performance [72]. These variations happen because of fluctuation in parameters at designing, fabrication and manufacturing level. Parameter variation causes degradation in overall circuit performance. Parameter variations increases at miniaturized technology nodes and cause various system integrity issues. As a circuit designer, the impact of variation in parameters need to be taken into account to improve performance and reliability [73]. These can be effectively performed using variability analyses.
Major challenge in subthreshold circuit designing is its very high sensitivity to process, voltage and temperature variations. This is due to the fact that current in subthreshold region is defined by exponential function that results in large deviation in output current due to small variations in any of the input parameters [73-73]. Three of the important variability analyses that have been conducted and presented in this paper are process corner, parametric and Monte-Carlo. These are described below. The effect of different varying parameter viz threshold voltage (V_{th}), effective gate length (L), oxide thickness (T_{OX}), supply voltage (V_{DD}) in IC have been considered.

7.1 Process corner analysis

Process corner analysis is used to analyze system performance at at different process corner modes. This helps to analyze several aspects of variabilities that occur during fabrication processes. This also facilitates in assessing circuit performance at worst possible conditions. The different process corners considered are Fast NMOS-Fast PMOS (FF), Slow NMOS-Slow PMOS (SS), Slow NMOS-Fast PMOS (SF), Fast NMOS-Slow PMOS (FS) and Typical NMOS-Typical PMOS (TT).

In the present work, power dissipation and delay are computed at different process corners [73, 74, 75, 76]. Power and delay are analyzed with varying temperature. Temperature is varied from -25^oC to 100^oC. Power dissipation and delay are computed as ratio of MLGNR to copper interconnects. If the value of this ratio is unity, then this signifies that both the copper and MLGNR interconnect have comparable performance. If MLGNR to copper ratio is higher than unity, it reflects that copper interconnects possess better performance than its counterpart MLGNR interconnect. However, in the other case (i.e. ratio lesser than unity) indicates that performance of MLGNR interconnect is superior than copper interconnect.

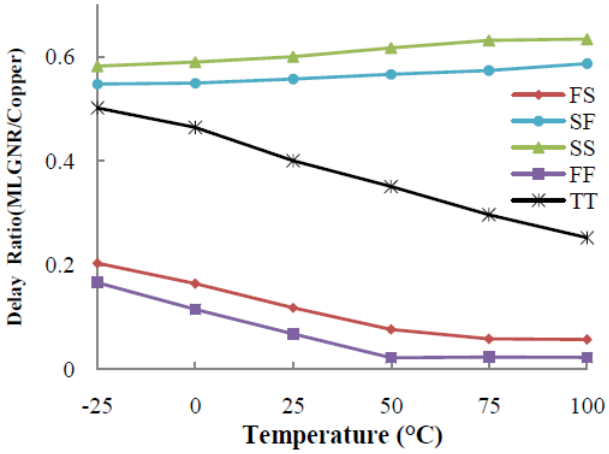

Figure 7.1: Delay analysis of graphene and copper interconnect with respect to temperature.

From Figures 7.1 and 7.2, it can be seen that the ratio of MLGNR to copper interconnect for both power dissipation and delay are lesser than unity. This convincely reflect that MLGNR interconnects possess higher performance. In Figure 7.1, it is seen that power ratio increases marginally with temperature. It is also analyzed that FF process corner model have the highest power dissipation while SS model has the least power dissipation. Figure 7.2 gives that delay variation with temperature at different process corners. Since FF model is characterized for fast operation, it results in lower delay in circuit.

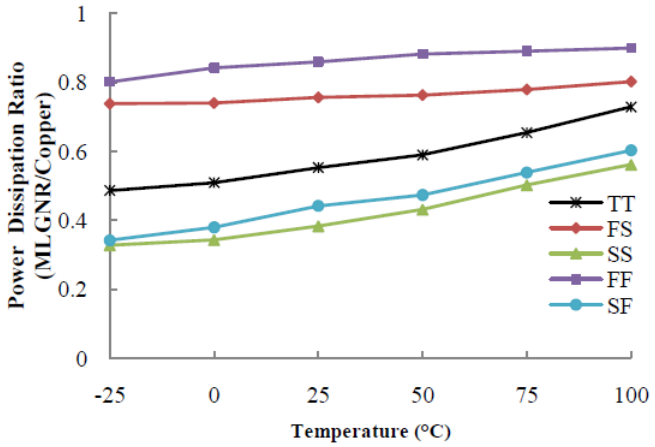

Figure 7.2: Power analysis of graphene and copper interconnect with respect to temperature.

7.2 Parametric sensitive analysis

Parametric sensitivity analysis deals with the variation of single parameter at a time. The considered parameters for analysis are threshold voltage (V_{th}), effective gate length (L), oxide thickness (T_{OX}) and supply voltage (V_{DD}). In this analysis, power dissipation and delay are computed by varying each of these parameters one at a time. Parameter variations are analyzed at 32nm technology node.

7.2.1 Threshold voltage (V_{th})

Threshold voltage variations occur due to dopant variations at the fabrication level [75]. The parameters are varied by $\pm 3\sigma$, where σ is the standard deviation for the Gaussian distribution function. The standard deviation for threshold voltage is taken as 12.5% [75]. The nominal value of threshold voltage at 32nm technology node of NMOS transistor is 0.5V. Power dissipation and delay are analyzed for copper and graphene interconnects as shown in Figure 7.3.
In Figure 7.3, it is seen that delay increases with increase in threshold voltage value. This is because as threshold value increases, the device switching time increases. This makes device slow. This is also evident from MOS drain current equation for subthreshold region given as stated in (2.7). From equation it can be defined that,

$$I_D \propto (V_{gs} - V_{th})^2 \tag{7.1}$$

Henceforth, for constant V_{gs} value, increase in threshold voltage value results in decrease in drain current. This indicates that device becomes slow as threshold

voltage increases. Consequently, delay in entire interconnect system goes on increasing with increase in threshold voltage. However the trend in power dissipation is opposite to the delay. For example, with increase in threshold voltage from 0.43V (-3σ) to 0.56V $(+3\sigma)$, power dissipation in graphene interconnect decreases from 70nw to 16.7nw and in case of copper interconnect, power dissipation decreases from 76.5nw to 21.6nw. It can be also analyzed from Figure 7.3 that graphene interconnect gives higher performance in terms of both delay and power dissipation that are lower than copper interconnects.

It is seen from the Figure 7.3 that graphene has lower delay and power dissipation compared to copper. It is seen that power dissipation at $\pm\sigma$ variation is 0.02uw and 0.064uw for graphene and copper interconnect respectively.

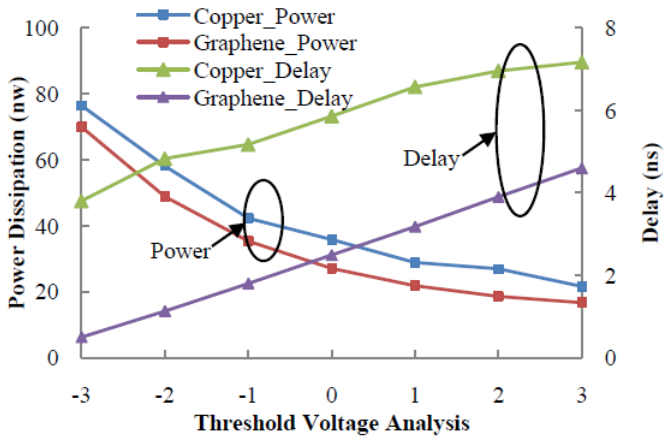

Figure 7.3: Delay and power dissipation analyses with threshold voltage variation.

7.2.2 Oxide thickness (T_{ox})

Oxide thickness variation generally occurs during device deposition and masking processes [53]. The $\pm 3\sigma$ percentage variation in oxide thickness has been taken as 4%. The nominal, minimum and maximum values of oxide thickness considered corresponding $\pm 3\sigma$ deviation are 1.65nm, 1.584nm and 1.71nm respectively. It is seen that increase in oxide thickness leads to delay increases as shown in Figure 7.4.

For example increase in oxide thickness from 1.65nm to 1.71nm results in 10.26% increase in delay. It can also be visualized from the Figure 7.4 that power dissipation decreases with increase in oxide thickness. For the same variation in oxide thickness, power dissipation decreases by factor of 5%.

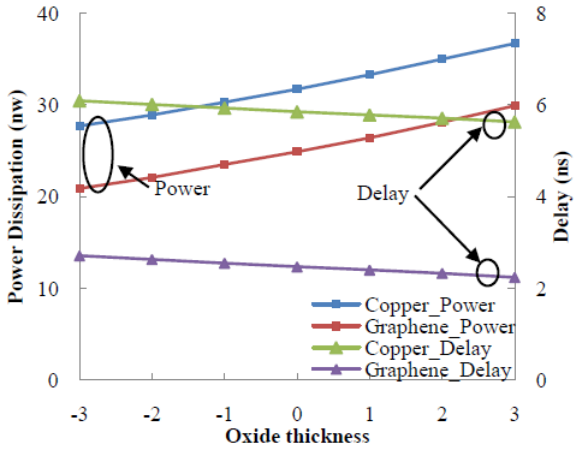

Figure 7.4: Delay and power dissipation analyses with oxide thickness variation.

7.2.3 Gate length (L)

Gate length variation occurs due to irregularities in lithography process. This results to various short channel effects in the devices [78-79]. The variation in gate length is taken as $\pm 15\%$ [76]. Power dissipation and delay are analyzed for copper and graphene by varying gate length and is shown in Figure 7.5. From

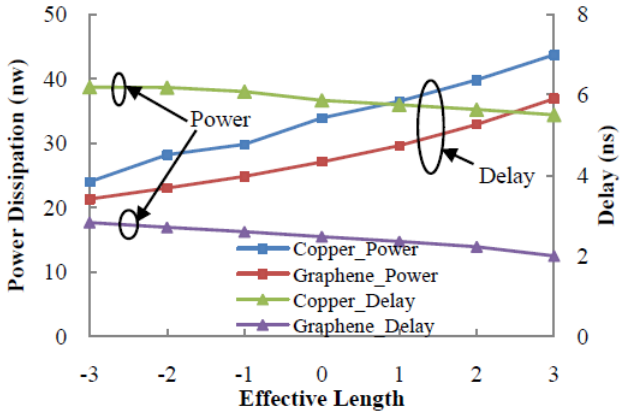

Figure 7.5: Delay and power dissipation analyses with gate length variation.

equation (2.7) is can be deduced that,

$$I_D \propto \frac{1}{L} \tag{7.2}$$

Hence, reduction in gate length leads to higher current. Higher current consequently leads to fast operation of device and system. This can be analyzed from Figure 7.5 that as gate length increases, delay increases and power dissipation

decreases. It is seen from figure that delay variation at $\pm 2\sigma$ is 2.8ns and 2ns for graphene.

7.2.4 Supply voltage (V_{DD})

Supply voltage variation can occur due to packaging irregularity and power fluctuations. For voltage variability analysis V_{DD} is varied by $\pm 10\%$ [76]. Voltage fluctuation causes switching voltage variation at the output node which in result causes fluctuation in delay and power dissipation. The interconnect can be modeled as inductance, capacitance and resistance. As supply voltage changes, current changes and correspondingly voltage drop across these parasitic element of interconnect also changes. These overall affects the system performance [73]. In Figure 7.6, variation in dissipation and delay are shown for copper and graphene interconnects by varying supply voltage.

From Figure 7.6, it is seen that power dissipation increases with increase in supply voltage. This is evident as higher supply voltage results in higher current through the device and interconnects. This results in more IV losses in the system. It is analyzed that power dissipation increases by 1.31 times as supply voltage change from 0.501V to 0.551V.

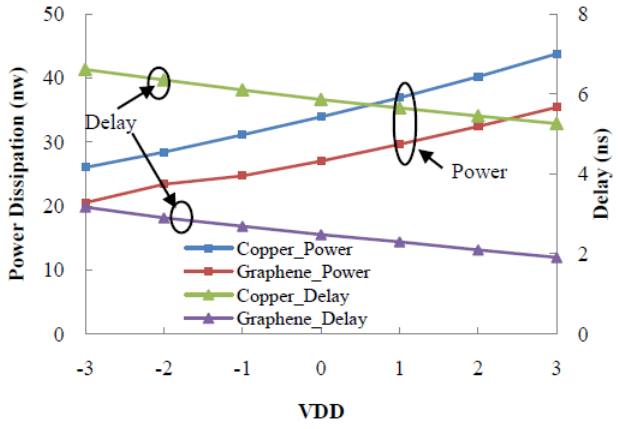

Figure 7.6: Delay and power dissipation analyses with supply voltage variation.

7.2.5 Interconnect parameters

Due to process and fabrication non uniformities, variations also occur in interconnect structures. The interconnect parameters considered for the variability analysis are:

(a) Variation in interconnect width (W),

(b) Variation in interconnect spacing (S),
(c) Variation in interconnect height (H), and
(d) Variation in dielectric thickness (T).
For example, during photo lithography and etching process, interconnect width and spacing varies. Intra-layer thickness and height varies due to deposition and chemical mechanical polishing (CMP) process [82].

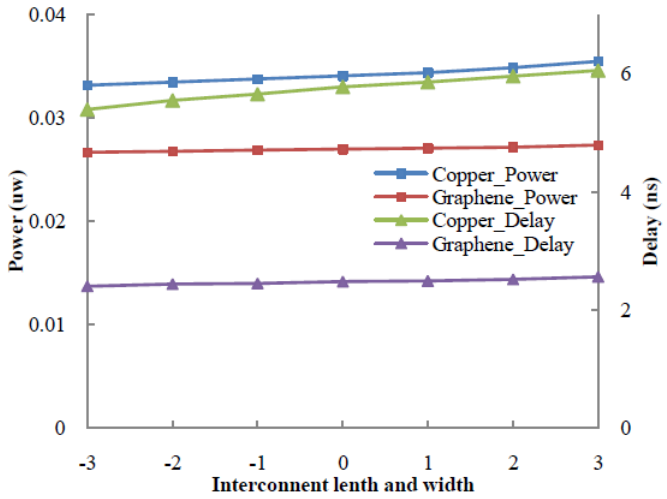

Figure 7.7: Delay and power dissipation analyses with interconnect parameter variation.

The interconnect parameters are varied as $\pm 10\%$ [76]. Parameters for interconnect are shown in Table 7.1. Power dissipation and delay for copper and graphene with varying interconnect parameters are shown in Figure 7.7.

Table 7.1: Values of interconnect parameters

Parameters	Nominal value	Minimum value	Maximum Value
Width (W)	250	225	275
Spacing (S)	250	225	275
Height (H)	585	526.5	643.5
Thickness (W)	375	337.5	412.5

7.3 Monte-Carlo analysis

In the Monte-Carlo analysis, all the parameters under consideration are varied simultaneously by $\pm 3\sigma$. In this analysis, power dissipation and delay are calculated by varying all the parameters together [77]. Monte Carlo analysis is used in order

to understand the effect of process variation on MLGNR interconnects. This analysis requires a large number of simulation trials. This is effective method to evaluate the performance of system under certain variations. For the analysis, 1000 runs have been considered. Probability distribution function (PDF) for propagation delay ad power dissipation derived by varying the parameters and is shown in Figures 7.8 and 7.9. Figure 7.8 shows that mean value of delay is 8ns. Figure 7.9 shows the power dissipation and the mean variation in the power dissipation is 0.3nw.

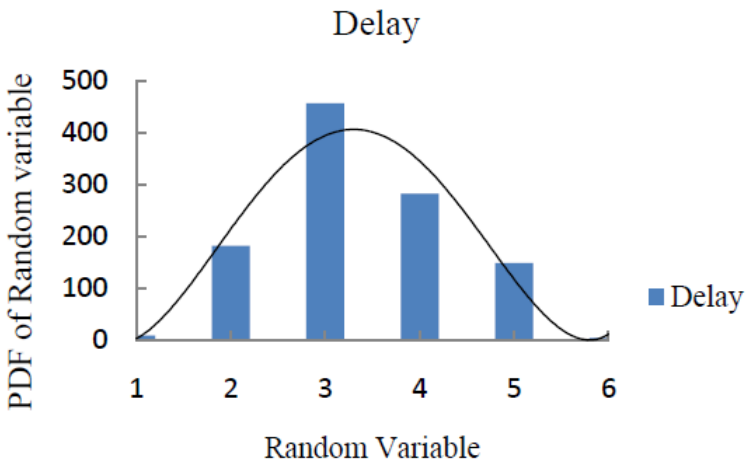

Figure 7.8: Probability distribution function for delay in Monte-Carlo simulation.

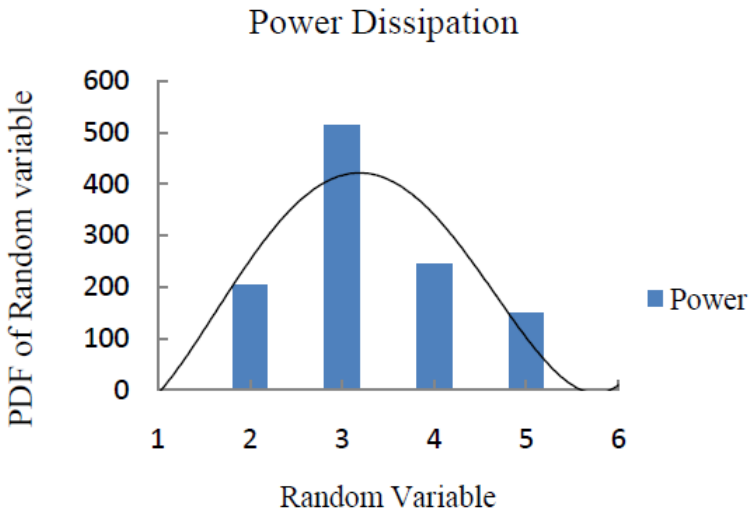

Figure 7.9: Probability distribution function for power dissipation in Monte-Carlo simulation.

CHAPTER 8
Conclusions

A detailed review of various interconnects and analysis of different materials have been presented. It is analyzed and seen that incorporation of interconnect material graphene enormously improves the system performance. As device dimension reduces, resistance, inductance and capacitance increases which leads to more power consumption, increased delay and cross talk effects. To reduce such problem different materials are used like graphene based CNTs and GNRs. GNR has been identified as one of the optimum solution for high-end performance in ICs.

Several mathematical and electrical models such as Elmore, two-port, numerical method and lumped, distributed, transmission line model are discussed. The demand for low power application has increased in portable e-circuits. Subthreshold region of operation helps for low power circuit designing. Present work innovatively analyses graphene interconnects in subthreshold region of operation. It is discussed that subthreshold region of operation is of prime importance for low power applications, while graphene interconnects is necessary for nanoscale technology nodes. For the effective analyses and comparisons, linear model and conventional copper interconnects have also been considered. This study has shown that MLGNR is better interconnect in terms of delay, power dissipation and PDP in both subthreshold and linear regions as compared to copper interconnect. The subthreshold modeling of graphene interconnects have been distinctly formulated using proposed FDTD based model. For the various analyze performed, it is analyzed that the proposed FDTD based model is highly accurate to the simulation model. It is seen that with subthreshold region of operation, power dissipation is nearly 26% lesser than linear region. Also PDP in subthreshold region of operation is nearly 3 times lower than linear region. Hence, subthreshold region of operation is good for low power applications. Consequently, it can be conveniently stated that graphene interconnects and its operation in subthreshold region shall be very prominent to meet ultra low power requirements in next-generation era. Variability analysis have also been performed. This analysis

gives the performance of overall system with respect to parameters variation. It is seen that graphene have better performance than copper interconnect.

List of Publications

1. N. Patel and Y. Agrawal, "A literature review on next generation graphene interconnect," *World Scientific Journal of Computer, Circuits and System*, Under Review.

2. N. Patel, Y. Agrawal and R. Parekh, "Novel subthreshold modeling of on-chip graphene using numerical method analysis," *IETE Technical Review Taylor and Francis*, Under Review.

3. N. Patel, Y. Agrawal and R. Parekh, "Variability analysis of on-chip graphene interconnect at subthreshold region," To be Communicated.

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