ASIC Chip Design For Healthcare System

by

Nishit Nathwani

202011064

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

in

INFORMATION AND COMMUNICATION TECHNOLOGY

to

DHIRUBHAI AMBANI INSTITUTE OF INFORMATION AND COMMUNICATION TECHNOLOGY

May, 2022

Declaration

I hereby declare that

(i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

(ii) due acknowledgement has been made in the text to all the reference material used.

Nishit

Signature of Student

Certificate

This is to certify that the thesis work entitled "ASIC Chip Design For Healthcare System" has been carried out by Nishit Nathwani (202011064) for the degree of Master of Technology in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology under my/our supervision.

Rutu M. Parekh

Dr. Rutu Parekh

Thesis Supervisor

Acknowledgement

First and foremost I am extremely grateful to my supervisors, Dr. Rutu Parekh for their invaluable advice, continuous support, and patience during my PhD study. Their immense knowledge and plentiful experience have encouraged me in all the time of my academic research and daily life. I would also like to thank Dr. Rutu Parekh for their technical support on my study. I would like to thank all the members in the our classmates. Finally, I would like to express my gratitude to my parents, Without their tremendous understanding and encouragement in the past few years, it would be impossible for me to complete my study.

Contents

Page No.

	Abstract	**iv**
	List of Principal Symbols and Acronyms	**v**
	List of Tables	**vi**
	List of Figures	**vii**
1	**Introduction**	**9**
1.1	General	9
1.2	Organization of Thesis	11
2	**Digital ASIC Design**	**12**
2.1	RISC-V ISA	12
2.2	Instruction Fetch (IF) Stage	12
2.3	Instruction Decode (ID) Stage	13
2.4	Execution (EXE) Stage	13
2.5	Memory Read (MEM) Stage	14
2.6	Write Back (WB) Stage	14
3	**Physical Design Flow**	**15**
3.1	Gate Level Netlist Stage	15
3.2	Floor Planning, Partition, and Power Planning	15
3.3	Placement, Clock Tree Synthesis	16
3.4	Routing, Timing Closure	17
4	**Analog ASIC Design**	**18**
4.1	CMOS Op-Amp Design	18
4.2	CMOS Comparator Design	18
4.3	Other Analog Components Design	21
4.4	Flash-type ADC Design	23
5	**Results Discussions and Conclusion**	**24**
	References	**32**

Abstract

We presents an application-specific integrated circuit (ASIC) implementation suitable for healthcare applications, which employ RISC-V as a digital processing unit and the sensor interfacing circuits. The motivation for improving living conditions day by day, sensors-based healthcare has been mostly used today era. SoC are used as monitoring tools for well-being or preventive purposes. Healthcare system with ultra low-power System on Chip (SoC) architecture specifically for wearable healthcare system, In order to reduce the power consumption of the processor, we design a ASIC that handles signal processing and provides computation The design consists of two sensors for collecting the force/pressure and ECG signal data. The design of analog circuits is done using the specifications obtained with these sensors. The data obtained can be processed with the computing device to extract information and take desired actions. The RTL-based design of a processor is implemented using Verilog HDL. Logic Equivalence is verified using Xilinx ISE. Physical realizations of the design are obtained using RTL to GDSII design flow. The analog design consists of unity gain buffer, sample and holds circuit, and flash type ADC. We have tested our ASICs with AMS verification methodology using Cadence CAD tools. Operating Frequency of overall system is observed 160 MHz and the area of digital core is 18088.380 μm^2 Total Power dissipation of the core is 368 μW operating Frequency of analog core is 4 MHz and and area is 468000 and power dissipation is 192.950 mW.

List of Principal Symbols and Acronyms

V_{TH}	Threshold Voltage
V_{dd}	Supply Voltage
S	Source
D	Drain
G	Gate
V_{ds}	Drain-to-Source Voltage
V_{gs}	Gate-to-Source Voltage
K_n or K_p	Device Trans-conductance
BW	Bandwidth
A_v	Gain
P_{diss}	Power Dissipation

Other minor symbols are defined at first occurrence; where necessary some symbols are redefined in the text.

CMOS	Complementary Metal Oxide Semiconductor
ASIC	Application Specific Integrated Circuit
DC	Direct Current
GaAs	Gallium Arsenide (Semiconductor Material)

List of Tables

		Page No.
Table 4.1	Two Stage CMOS Op-Amp Specifications	18
Table 4.2	Op-Amp Each MOSFET's W/L Ratio	20
Table 4.3	Comparator Each MOSFET's W/L Ratio	22
Table 5.1	Specification Obtained	30
Table 5.2:	Comparison With Others work Digital ASIC Design	30
Table 5.3:	Comparison With Others work Analog ASIC Design	31

List of Figures

		Page No.
Figure 1.1	Block Diagram of Proposed Healthcare System	11
Figure 2.1	Instruction Fetch Stage	12
Figure 2.2	Instruction Decode Stage	13
Figure. 2.3	Execution Stage	13
Figure. 2.4	Memory Read Stage	13
Figure. 2.5	Write Back Stage	14
Figure. 3.1	Physical Design Flow	17
Figure. 4.1	Two Stage CMOS Op-Amp Design	19
Figure. 4.2	Two Stage CMOS Comparator	22
Figure. 4.3	Unity Gain Buffer (UGB)	24
Figure. 4.4	Sample And Hold Circuit	24
Figure. 4.5	Flash-type ADC Structure	25
Figure. 5.1	Functionality Verification of RISC-V Core	27
Figure. 5.2	Final Layout of The RISC-V Core	27
Figure. 5.3	Transient Simulation of Op-Amp	28
Figure. 5.4	AC Analysis of CMOS Op-Amp	28
Figure. 5.5	Transient Simulation of CMOS Comaparator	28
Figure. 5.6	Transient Simulation of UGB	29
Figure. 5.7	Transient Analysis of Flash-Type ADC	29
Figure. 5.8	Final Layout of Analog ASIC Design	32

Chapter 1
Introduction

1.1 General

With improving living conditions day by day, sensors-based healthcare has been mostly used today era for highly accurate results. Embedded systems including SoC based designs are used as monitoring tools for well-being or Decision oriented. Such systems are composed of non-invasive and wearable sensors with high speed processors [1]. Currently, machine learning and edge computing are widely used for various applications in diverse fields, and health care is no exception, It can be used to improve the accuracy of monitoring, quick analysis, which is a popular method in the wearable technology [2]. Repeatedly monitoring of routinely based collected data to improve the timely diagnosis in accurate respiratory distress syndrome, especially of frequently under-diagnosed mild stages as well as to increase guideline process where good precision healthcare system needed [3]. Need a healthcare system with ultra low-power System on Chip (SoC) architecture specifically for wearable healthcare devices, In order to reduce the area and power consumption of the processor, we design a hardware accelerator that handles signal processing and provides computation off loading. Furthermore, to minimize the area, power and maximize the performance of the accelerator [4]. There are various platforms available now for ECG signal processing such as a microprocessor, microcontroller, Personal Computer (PC), mobile phone, and digital signal processor. However, they have their own drawbacks in ECG signal processing. For example, a microprocessor-based system with discrete component system limited in performance by clock speed and complexity of its internal design. Sequential nature is the fetch-decode-execute cycle in microcontroller which is a time-consuming process in handling instruction [5].

Now a day from rapid technology advances in signal processing with edge computing, biomedical sensing, and ASIC with optimize performance [7-8]. We need low-power ECG signal processing ASIC chip design with extract the ECG features for wearable health devices systems. The new trends are used for the diagnosis of ECG arrhythmia by using artificial intelligent features. We need

design consists of an sensing unit, analog to digital conversion, pre-processing stage, and feature extraction stage for information decision. Combinational both analog and digital ECG data computing device in single ASIC [9]. Currently, the Internet of Things (IoT) and supporting technologies such as cloud computing and big data analytics are helping us to shift the clinic-centric approach to the person-centric model or personalized healthcare system [11].

One flash-type analog-to-digital converter (ADC) was realized by a mixed-signal application-specific integrated circuit approach (ASIC) [12]. With the availability of the Internet-of-things and Internet-of-Everything provide facility to device connected world through VLSI technology, with the help of CMOS-enabled technology possible. There is enormous potential for microfluidic technologies in affordable healthcare system technology for everyone, and CMOS technology will play a major role in making that happen through ASIC design [15-16].

Need of fully integrated application-specific integrated circuit (ASIC) sensor for the recording of multiple bio-electric signals and process it through trending technology [17-18].

The top module of the design is shown below Fig.1, where the designed ASIC modules are placed to build one complete SoC of the Healthcare System. The figure shows the top-level diagram of the implementation. RISC-V Core build using RV32I ISA. Instruction memory contains the program that must be executed. It is unidirectional memory. Data Memory includes the data that we load or store in memory. Data Memory is bidirectional. These implementations are in the Digital domain (RTL to GDSII). ADC(Analog to Digital Converter) and Sensor interfacing circuitry are analog components. The ADC is used for the sensors for digital outputs. The following sections have detailed information on all the implementations done, where starting from digital ASIC design which is consists of it's RTL design and it's physical design flow. After that Analog ASIC design which is consists of CMOS Two stage Op-Amp, CMOS open-loop comparator, Sample and Hold circuit, Unity gain buffer, etc…

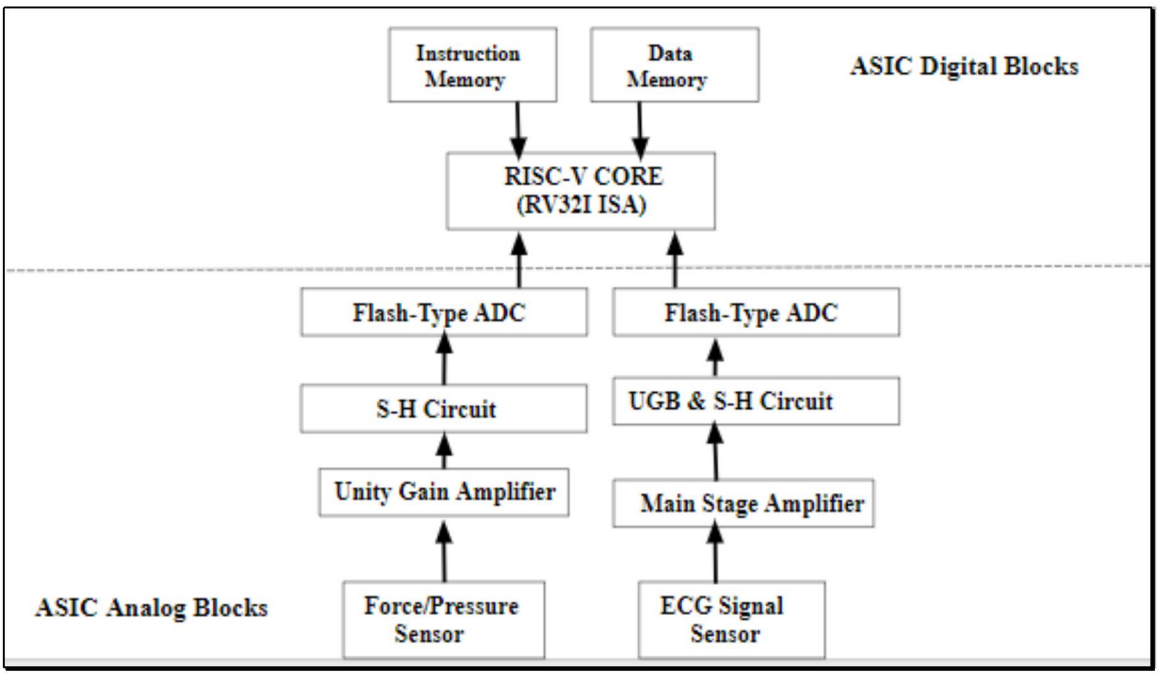


Figure. 1.1 Block Diagram of Proposed Healthcare ASIC System

1.2 Organization of the Thesis

From the next in chapter 2 we have explained detailed implementation strategy starting from Digital ASIC Design implementation which is consists of RISC-V microprocessor core, Instruction and Data Memory. Chapter 3 is about physical design flow, on which I have explained how we can tap-out our digital ASIC design and how our design passed the entire flow from scratch. Chapter 4 contains information regarding Analog ASIC Design implementation starting from CMOS Op-Amp, Comparator, Unity gain buffers, and 6 bit Flash-type ADC. In the Chapter 5 I have discussed about the simulation results and analysis of both of the ASICs. At last we have completed our work with future scope and further improvement possibilities.

Chapter 2
Digital ASIC Design

2.1 RISC-V ISA

RISC-V is an open source standard instruction set architecture (ISA) based on the established reduced instruction set computer principle. RISC-V is a five stages pipelines architecture namely Instruction Fetch Stage (IF), Instruction Decoder Stage (ID), Execution Stage (EX), Memory Access Stage (MEM), Write Back Stage (WB). Here I have designed a micro-architecture of the RV32I base version of the ISA which consists of the 35-40 Instructions. Complete functionality was designed using Verilog HDL and the complete design was made synthesize for physical design flow.

2.2 Instruction Fetch (IF) Stage

The next instruction is fetched from the memory address that is currently stored in the program counter and stored into the instruction register. At the end of the fetch operation, the PC points to the next instruction that will be read at the next cycle. So IF stage instruction fetched and Program Counter (PC) is incremented by plus 4 as shown in Figure 1.2.

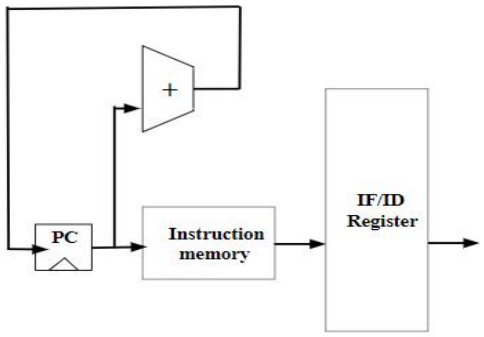


Figure. 2.1 Instruction Fetch Stage

2.3 Instruction Decode (ID) Stage

During this stage, the encoded instruction presented in the instruction register is interpreted by the decoder. In the ID stage, if the instruction in the IR is not a jump (j, jal, or jr), the CPU performs the reading sources operands from the register file or generates a Sign extended immediate or offset values calculation and applies to the execution EX stage as shown in Figure 1.3.

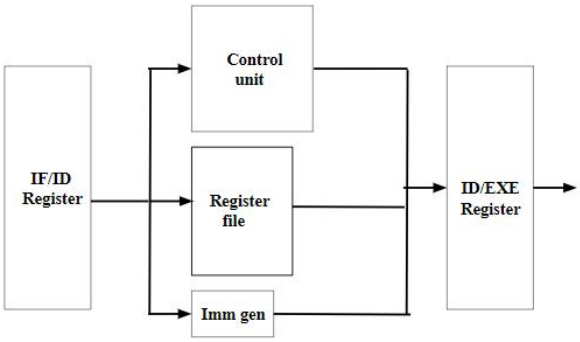


Figure. 2.2 Instruction Decode Stage

2.4 Execution (EXE) Stage

Where Either R-type instruction is performed inside the ALU and updated the required flags or effective addresses for branch, load-store, and jump type instructions are also calculated inside the same blocks by differentiating ALU-src and ALU-op architectural view shown in Figure. 1.4.

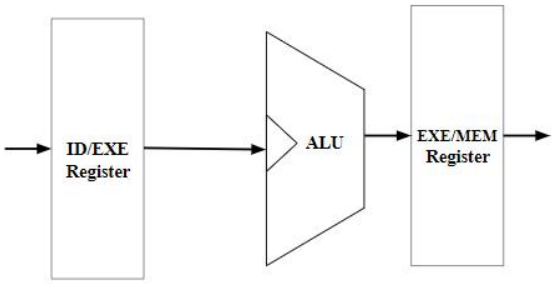


Figure. 2.3 Execution Stage

2.5 Memory Read (MEM) Stage

The load and store instructions are affect this stage, at this stage come into the picture where data memory access for data transfer the blocks which are used out of the complete data path are shown Figure. 1.5.

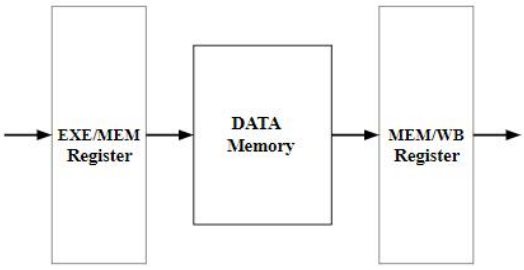


Figure. 2.4 Memory Read Stage

2.6 Write Back (WB) Stage

For all the instructions where the final destination register where this stage write the results inside the destination register which is detected at the instruction decoder stage. Normally R-type/Load-type/J-type instructions will be affecting this stage and it's micro architecture are shown in Figure. 2.5.

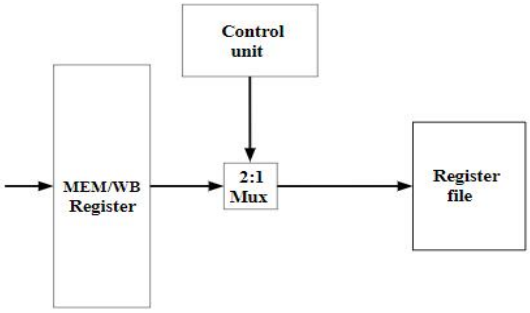


Figure. 2.5 Write Back Stage

Here I have design micro architecture such a way that it is detect hazards using hazard detection unit if any occurred either read after write (RAW) or write after write (WAW) then it's stall the normal operation of the microprocessor. Normally hazards stops execution and give wrong calculation results. Here I have design entire micro-architecture using Verilog HDL and made it synthesize for ASIC physical design implementation.

Chapter 3
Physical Design Flow

3.1 Gate Level Netlist Stage

The files required for the Netlist stage are mentioned below.
i) Gate level Netlist:
A synthesis tool will translate RTL into a collection of interconnected logic gates that define the logic. The most common format is Verilog.

ii) Standard Cell Library:
Standard Cell Library will have a layout model and timing model information for the Standard cells.

iii) Technology file:
The rules about the process that has been selected should also be given to the PNR tool. This includes metal widths, spacing, definitions, etc.

iv) Timing Constraints:
SDC files define the timing constraints of your design. You will have the clock definitions, false paths, any input and output delay constraints, etc.

3.2 Floor Planning, Partition, and Power Planning

This is the first significant step for the layout. The floor plan determines chip quality. Here, we define overall the size of the chip/block, allocating power routing resources, place the hard macros, and reserve space for standard cells. Every subsequent stage, like placement, routing, and timing closure, is dependent on how good the floor-plan defined. In a real-time design, we go through many iterations before you arrive at an optimum floor-plan. The main steps for this stage are given below.
i) Core Boundry:
The floorplan defines the size and shape of your chip/block. The Floorplanning can be controlled by various parameters like Aspect Ratio, Core utilization, Boundry.

ii) IO Placement/Pin Placement:
We need to place IO pads and IO buffers on the chip. We will also get a maximum and minimum die size according to the package.

iii) Macro Placement:
Once the size & shape of the floorplan are ready, we can place macro. The creation of the power Rings and straps happens in this step.

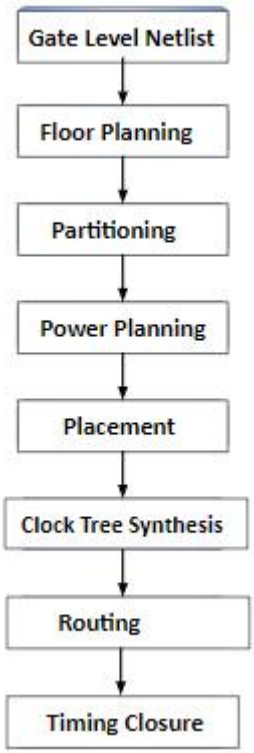


Figure. 3.1 Physical Design Flow

3.3 Placement, Clock Tree Synthesis

Standard cell placement happens in this stage after Floor-planning, i.e., creating the core area, placing the macros, and deciding the design's power network structure. The tool optimally determines the location of each of the components on the die at this stage. Various factors like the timing analysis of the system including interconnect lengths and hence the connections between standard cells, power dissipation, etc. Placement also determines the reputability of our design. It also optimizes the design, thereby removing any timing violations created due to the relative placement on a die.

After placement, we have positions of all the cells, including macros and standard cells. At this stage, buffer insertion, gate sizing, and any other optimization technique are employed on the data paths, but no change is made to

the clock net. We want a "balanced" tree; that is, the skew value for the clock tree should be zero, which happens in the clock tree synthesis step.

3.4 Routing, Timing Closure

After CTS, the routing process determines the precise paths for interconnections, including the standard cells and hard macro pins, the pins on the block boundary, or pads at the chip boundary including I/O port. In the routing stage, metal and vias are used to create the electrical connection in layout to complete all connections defined by the netlist. The order of routing is Power routing, Clock Routing, and Signal Routing. At the timing closure final optimizes circuit performance by specialized placement or routing techniques.

Chapter 4

Analog ASIC Design

Analog ASIC contains sensor interfacing circuit starting from Op-Amp, Unity gain buffer (UGB), Sample And Hold, Flash type ADC, etc.. Here below section explain detailed explanation and analysis of individuals components and entire Analog ASIC system.

4.1 CMOS Op-Amp Design

An operational amplifier (Op-Amps) is an integrally part of many analog and mixed-signal circuit designs. Op-amps with different levels of complexity are used to design ranging from dc bias generation to high-speed amplification or filtering applications. The design of an op-amp is to pose a challenge as the supply voltage and transistor channel lengths scale down with each technology generation of CMOS tech node.

Here I have a design op-amp based on the specification which is matched the Sample and Holds as well as ADCs circuit design parameters. Our designed op-amp specifications are mentioned in Table 1.

From the specifications, there is a standard two-stage CMOS op-amp design methodology and verify functionality. Two-stage op-amp which basically consists of the first stage is that differential amplifier and the second stage is common source amplifier as shown in the below Figure. 4.1.

CMOS Operational amplifier has a standard design which is shown below whereas and every specification is related to each and every MOSFET parameter. I have designed an Op-Amp Using gpdk 180nm which is provided inside the cadence virtuoso as shown in the below figures where each MOSFET's have channel length is 500nm because the channel length modulation is avoided.

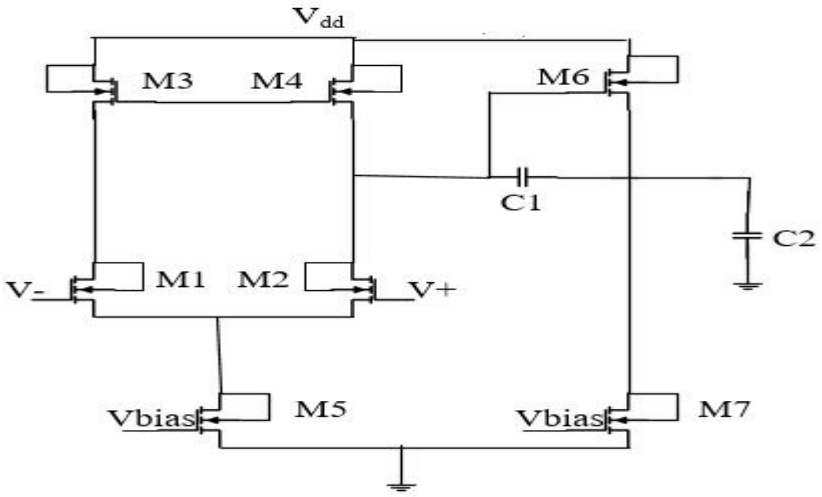


Figure. 4.1 Two Stage CMOS Op-Amp Design

TABLE 4.1- Two Stage CMOS Op-Amp Specifications

Sr. No.	Design Parameter	Values
1	Supply Voltage	1.8 V
2	Biasing Current	16 μA
3	Open-loop Gain	70-75 dB
4	Gain-Bandwidth Product	10 MHz
5	Slew Rate	10 V/μs
6	ICMR	0.8 to 1.6
7	CMRR	>60 dB
8	PSRR	>60 dB
9	Output Swing	It depends upon the load
10	Power Dissipation	<1 mW

For the designing of a two-stage CMOS Op-amp various design steps need to be considered. These design steps help to achieve the proper sizing of the transistors used in an CMOS op-amp. It has been assumed that all the transistors are in a saturation state.

Then we choose the device length to be used throughout the circuit which keeps the channel length modulation parameter constant. Below are the steps for designing a two-stage CMOS op-amp.

For the desired phase margin (PM) of 60 degrees, choose the the value of Cc by assuming z ≥ 10 GB using the equation,

$$C_c > 0.22C_L$$

Determine the tail current I_5 using the equation as shown below,

$$I_5 = SR.\, C_c$$

Design for M1 from maximum input voltage specifications, given by the equation

$$\left(\frac{W}{L}\right)_3 = \frac{I_5}{(K_3)\{V_{dd} - V_{in}(max) - V_{t03}(max) + V_{t1}(min)\}^2}$$

We verify that the pole and zero due to Cgs_3 and Cgs_4 will not dominate by assuming $P_3 > 10$ GB,

$$\frac{gm_3}{2 \times C_{gs_3}} > 10.GB$$

Design for M1 and M2 so as to achieve desired GB

$$gm_1 = GB.C_c$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{(gm_2)^2}{K_2.I_5}$$

Design for M5 by first calculating V_{ds5}(sat) as given by below equation,

$$V_{ds5}(sat) = V_{in}(min) - V_{ss} - \frac{I_5}{B_1} - V_{t1}(max) \geq 100mV$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{(K_5[V_{ds5}(sat)^2]^2)}$$

Design for S6 by letting $p_2 \geq 2.2.GB$

$$gm_6 = 2.gm_2(^{C_L}/_{C_c})$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 (^{gm_6}/_{gm_4})$$

Now we solve for I6 as given by the equation

$$I_6 = (^{gm_6{}^2}/_{2K_6S_6})$$

Design for S7 as given by the equation

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 (^{I_6}/_{I_5})$$

Check for gain and power dissipation as given by equation,

$$A_v = 2gm_2gm_6/\{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)\}$$

$$P_{diss} = (I_5 + I_6).(V_{dd} + V_{ss})$$

TABLE 4.2- Op-Amp Each MOSFET's W/L Ratio

M1,M2	2
M3,M4	10
M5,M8	44
M6	48
M7	100

Each MOSFET's W/L ratio is calculated from the standard design equations which are shown in Table 2. Taken L_{eff} = 500nm. Frequency analysis and the transient analysis are shown in Fig. 5 and Fig. 6 with input is sinusoidal signal.

4.2 CMOS Comparator Design

The comparator is a circuit that compares an two analog signal with another analog signal or reference and outputs a binary signal based on the comparison results.The comparator is mostly used in the process of converting analog signals to digital convertor. In the analog-to-digital conversion process, it is necessary to first sample the input which is followed by UGB. This sampled signal is then applied to a pairs of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog–digital converter. CMOS open-loop comparator is shown in the below Figure. 4.2.

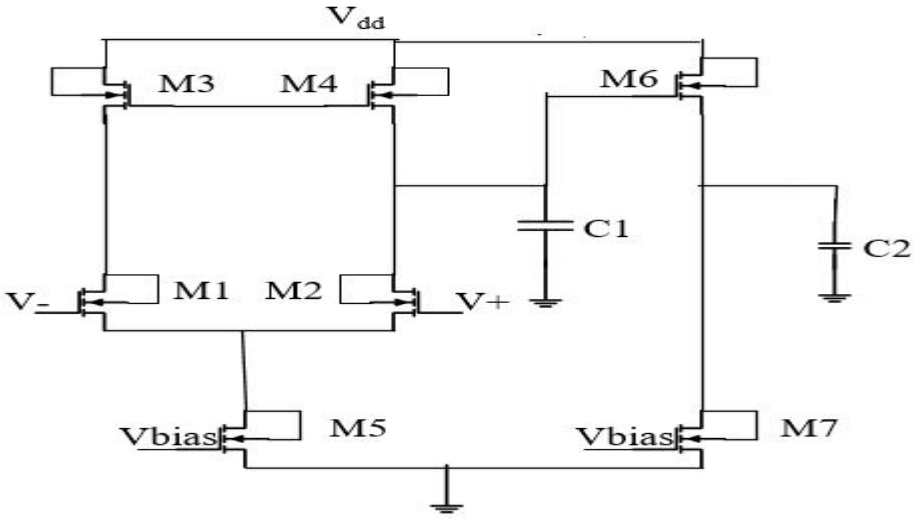


Figure. 4.2 Two Stage CMOS Comparator

CMOS comparator is also designed based upon standard equation which are given below,

$$|PI| = |PII| = \frac{1}{tp\sqrt{mk}}$$

$$I_7 = I_6 = \frac{|PII|CII}{\Delta n + \Delta p}$$

$$\left(\frac{W}{L}\right)_6 = \frac{2.I_6}{K_6(V_{ds6}(sat))^2}$$

$$\left(\frac{W}{L}\right)_7 = \frac{2.I_7}{K_7(V_{ds7}(sat))^2}$$

Guess CI as 0.1-0.5 pF ; $I_5 = I_7.2CI/CII$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{K_3(V_{gs3} - V_{tp})^2}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(gm_2)^2}{K_2.I_5}$$

$C1 = Cgd_2 + Cgd_4 + Cgs_6 + Cbd_2 + Cbd_4$

$$V_{ds5}(sat) = V_{icm}(-) - V_{gs1} - V_{ss}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{(K_5[V_{ds5}(sat)^2]^2)}$$

TABLE 4.3- Comparator Each MOSFET's W/L Ratio

M1,M2	8
M3,M4	10
M5,M8	15
M6	272
M7	136

4.3 Other Analog Components Design

Now another components such as unity gain buffer (UGB) and sample and hold are required before designing the entire flash-type ADC. In this section I have provide it's detail information with design equations. Figure. 4.3, show the diagram of unity gain buffer which is designed by using high gain operational amplifier.

Here below figure work as unity gain because we know standard equation of the non-inverting Op-Amp which is given below,

$$V_{out} = (1 + \frac{R_f}{R_1})V_{in}$$

If R_f and R_1 is zero then Vout =Vin

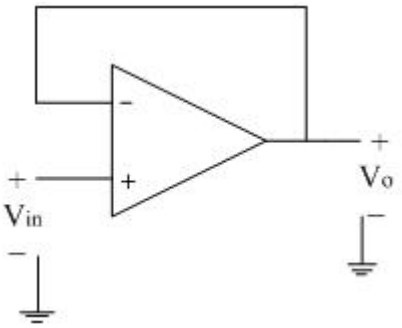


Figure. 4.3 Unity Gain Buffer (UGB)

Similarly sample and hold circuit using high gain operational amplifier as shown in Figure. 4.4, where two op-amp along with one NMOS switch for controlling operation and hold capacitor. In this configuration when the NMOS switch is on hold capacitor start to charge and when off then capacitor hold charges and transfer to the last unity gain amplifier. As there is no feedback, this circuit is relatively faster than the coming circuits. But the feedback in the closed-loop architectures provide higher accuracy figures. The acquisition time must be as low as possible. It is dependent on three factors: 1.The RC time constant, where R is the ON resistance of the MOSFETs and holding capacitor CH. 2.Maximum output current. 3. Depends upon Slew-rate of the Op-Amp.

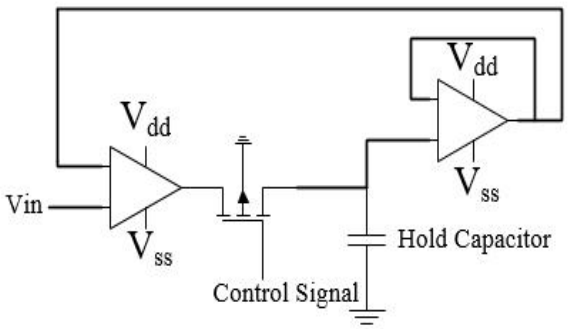


Figure. 4.4 Sample And Hold Circuit

4.4 Flash-type ADC Design

Here I have targeting flash-type ADC because it's optimize in terms of speed and area based than other architectures. As shown in Fig. 8 is structure of ADC which consists of array of the comparator, and then priority encoder.

For AMS verification cadence tools provide facility to verify functionality using it's standard methodology in which I have designed 64 to 6 priority encoder using Verilog HDL and create it symbol and then designed entire ADC structure and verified it's functionality simulation as shown in Figure. 5.1. Similarly we have tested for various input sample values to verified it's logical equivalence and functionality of expectation. Here I have targeted Flash-Type ADC because it's optimized in terms of speed, power and Area which are performance factors. Here I have designed 6 bit for exploration methdology for ASIC implementation as well as AMS design implementation.

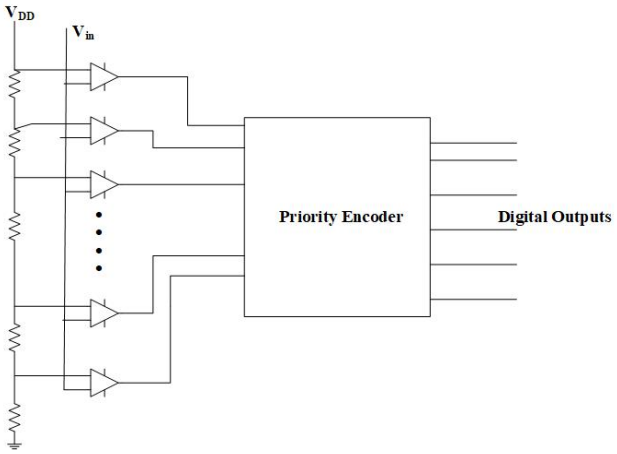


Figure. 4.5 Flash-type ADC Structure

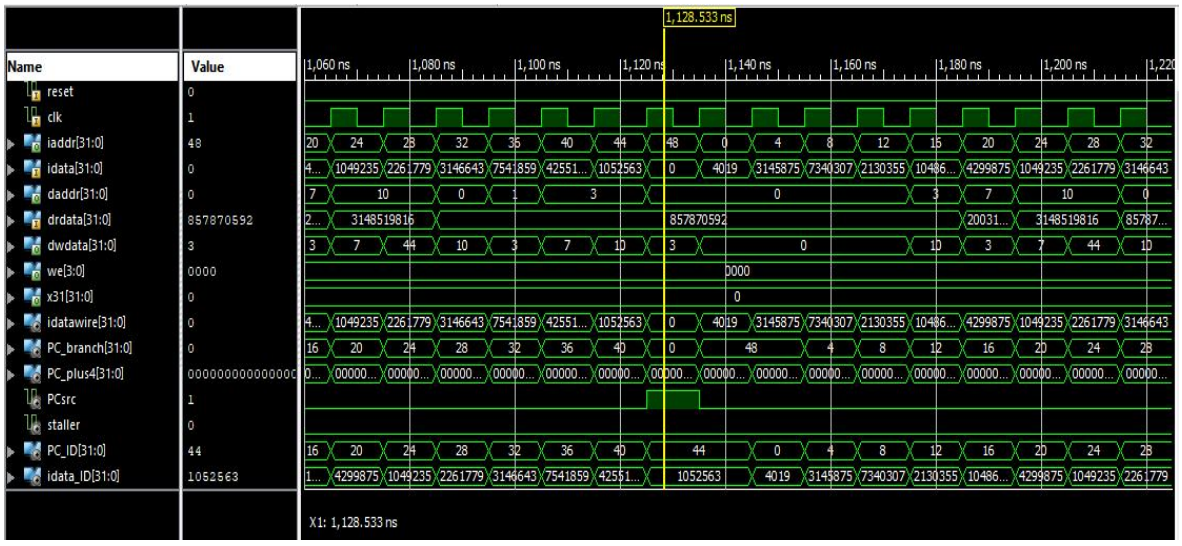
After designing individuals components now we have assembled together as per above block diagram so here I have designed 6 bit ADC based upon the precision that we need to required for proper sensor interfacing. Here we have verify the functionality of the ADC by using cadence AMS verification mythology which is shown in the results section.

Chapter 5

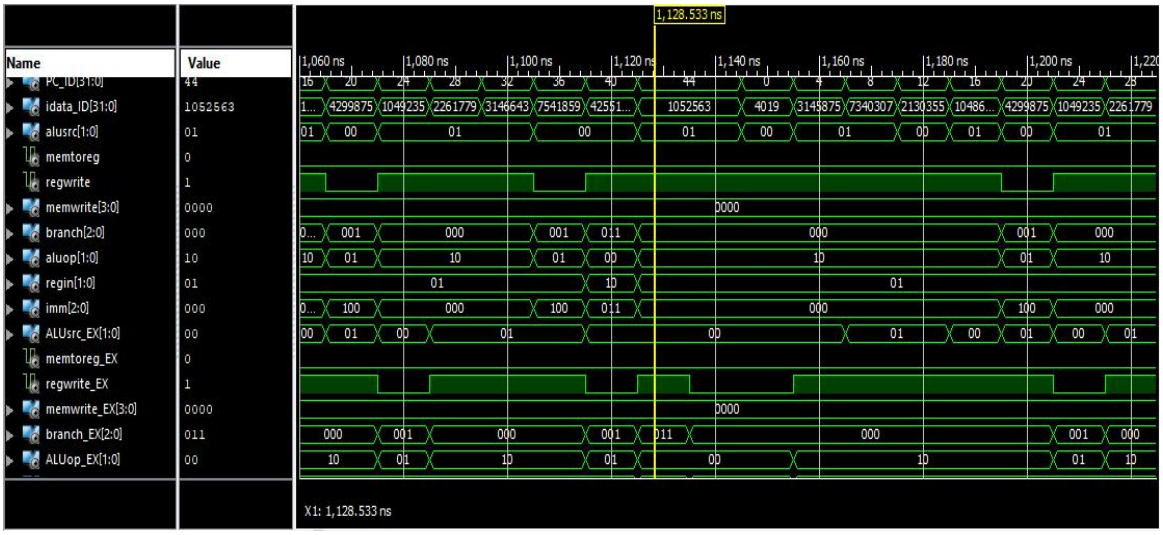
Results Discussions And Conclusion

First we have verified functionality of the RISC-V ISA and check it's logical equivalence using Xilinx ISE shown in below Figure. 5.1(a,b), here we have made two memory module for testing purpose where written few combinations of the instructions along with data memory so we have verified overall computation results which are as expected. After completed functional simulation we were implemented it's complete PD flow using Cadence tools (Genus/Innovus), where we have performed pre-synthesis and post-synthesis analysis to verified final layout of the core as shown in Fig. 10. As performance parameter results are shown in Table- 5.1.

After starting of the analog ASIC is from the Op-Amp, so as shown in Figure. 5.3 and 5.4 about it's transient simulation and frequency response. AC analysis of the opamp with capacitive load is shown in the below figure where DC gain is obtained 70-75 dB and phase margin is 62.5^{o} as per the specification. Similarly open loop two stage CMOS comparator is design, so it transient simulation is shown in Figure. 5.5. For Flash-Type ADC we need Sample And Hold (S-H) circuit along with unity gain buffer who provide current driving capability. Their simulation results are shown in Figure. 5.6. All Analog system layouts are also generated and verified so that are shown in Figure. 5.8 complete ADC with Two-stage CMOS Op-Amp, Comparator, Unity gain buffer, and sample and hold circuit.



(a)



(b)

Figure. 5.1 Functionality Verification of RISC-V Core

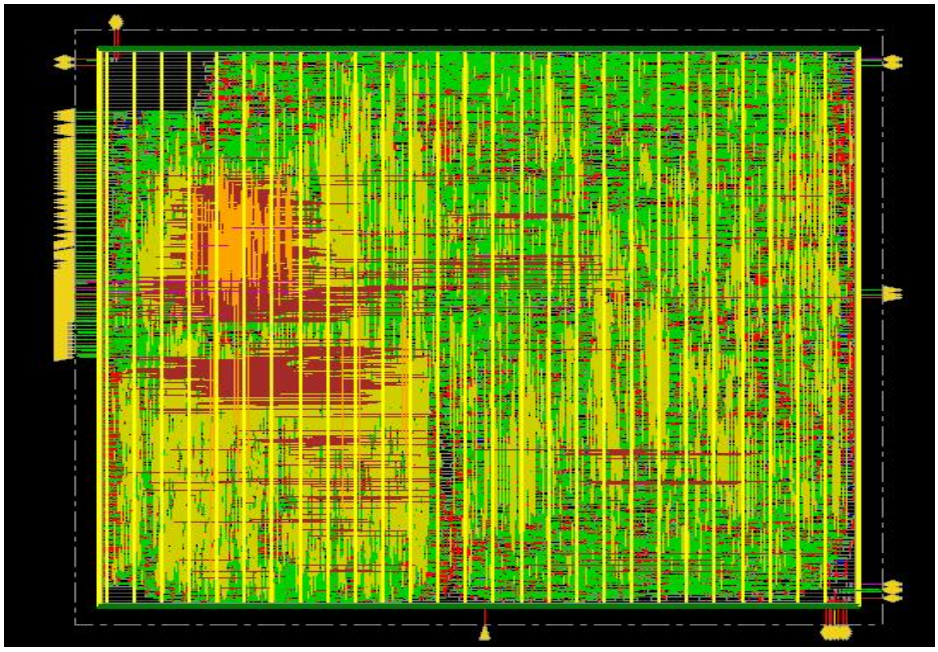


Figure. 5.2 Final Layout of The RISC-V Core

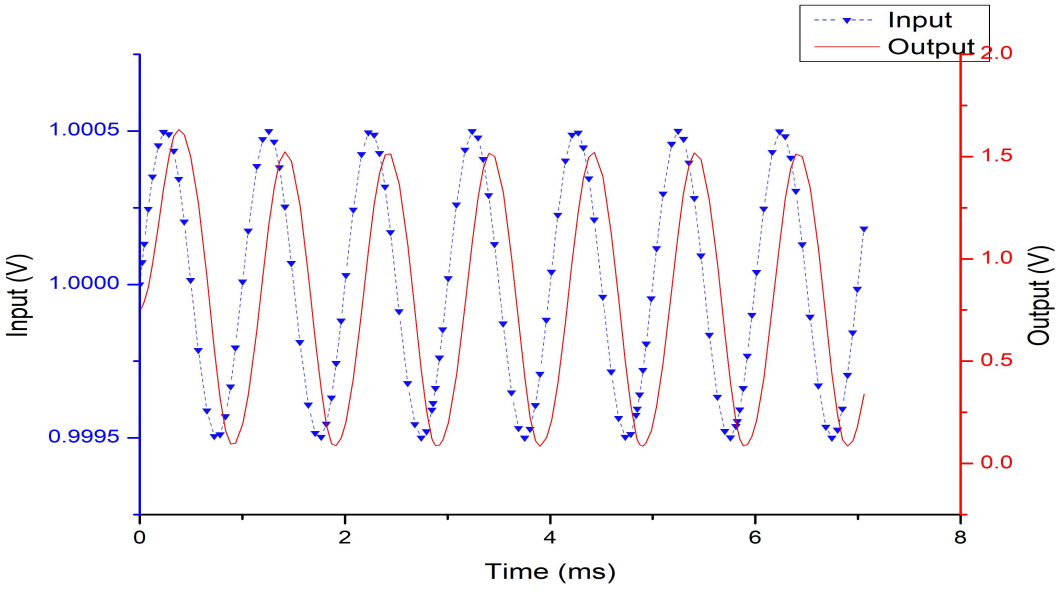


Figure. 5.3 Transient Simulation of Two Stage Op-Amp

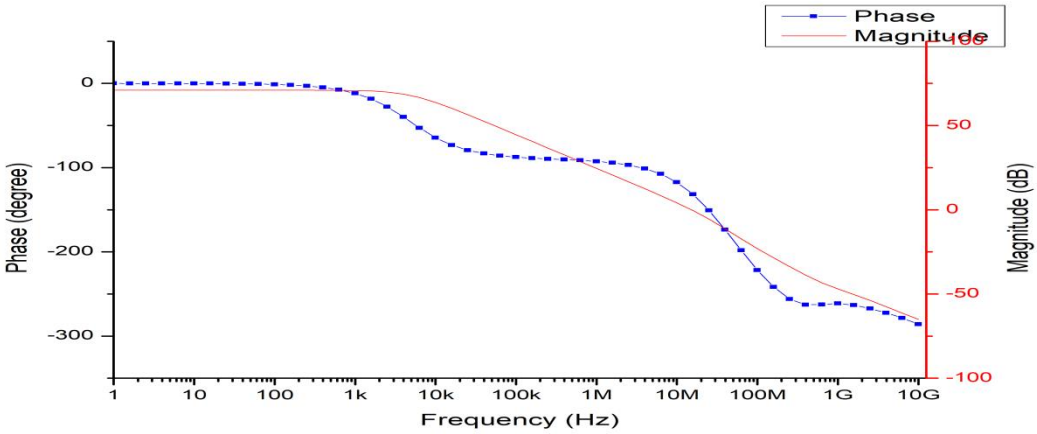


Figure. 5.4 AC Analysis of CMOS Op-Amp

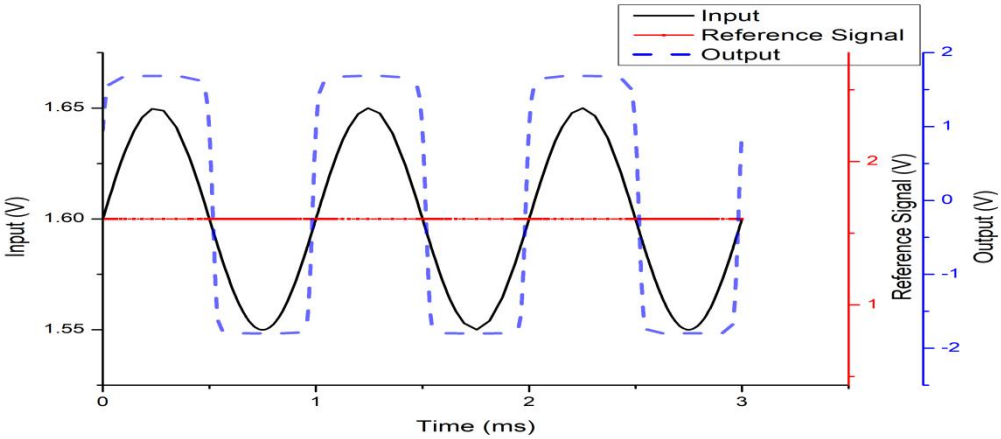


Figure. 5.5 Transient Analysis of CMOS Comparator

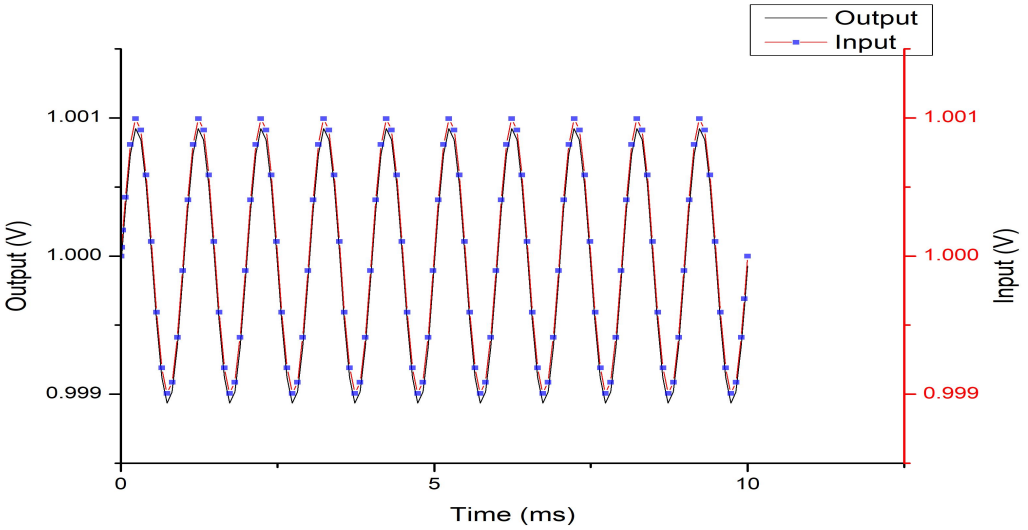


Figure. 5.6 Transient Simulation of Unity Gain Buffer

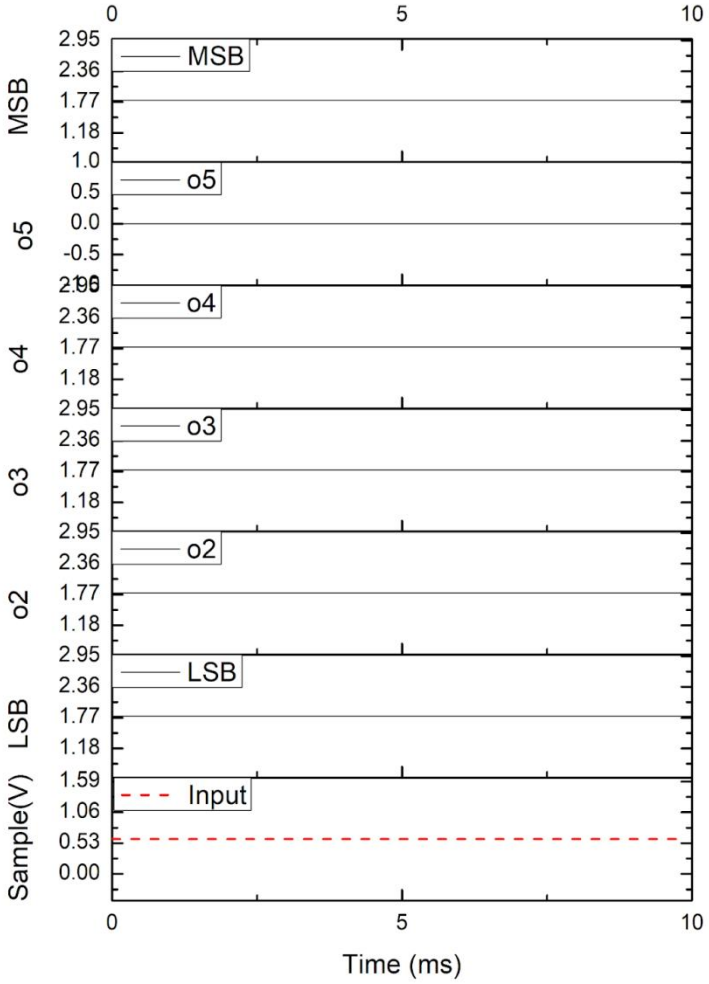


Figure. 5.7 Transient Analysis of Flash-Type ADC

Future healthcare will become largely dominated by electronics. The transition from hospital-based care, through home care and consumer wearable, is only possible by the innovations in IC design. Chips become smarter, smaller, faster, and can run longer on a single battery with demanding the use of ASIC. Here I have designed separate ASIC for digital system blocks and it's functionality of logic equivalency and after that it's physical design flow using cadence tools kit (Genus, Innovus, Tempus), and design analog system blocks components and it's simulation and after that layout of the individual blocks as well as whole system layout design using cadence tool kit(Virtuoso, Layout XL, AMS verification). Due to RISC-V ISA, it will be able to perform the machine learning algorithms for the sensor's processing. As we have used multi technology node design approach because we have design digital ASIC design on 45nm technology node and analog ASIC design on 180nm technology nod. So our proposed ASICs will enable us to design SoC with include higher level of the functionality including IoTs for wireless transmission.

Table 5.1: Specification Obtained

Parameter	**Digital ASIC**	**Analog ASIC**
Area(μm^2)	18088.380	468000
Frequency(MHz)	2850	4
Power Dissipation(μW)	368	192,960

Table 5.2: Comparison With Others work Digital ASIC Design

Sr. No.	This Work	[12]	[13]	[14]	[15]
Technology	45nm	65nm and 130nm	130nm	FPGA	FPGA
Instruction Set	RV32I	RV32I	RV32IMC	RV32I	RV32I
Pipeline Stages	5	5	5	5	5
Area (μm2)	18088.380	-	200000	-	-
Power (μW)	368	600	500	2650	4500

Table 5.3: Comparison With Others work Analog ASIC Design

Sr. No.	This Work	[16]	[17]	[18]
Technology	180nm	180nm	180nm	180nm
Gain Bandwidth (MHz)	10	30	34	-
Gain(dB)	72	67.5	65	-
Power (μW)	550	600	500	2650
Propagation Delay(ns)	250	-	-	300
Phase Margin	62.5	60	65	-

Layout of Sample & Hold Circuit

Layout of Unity Gain Buffer

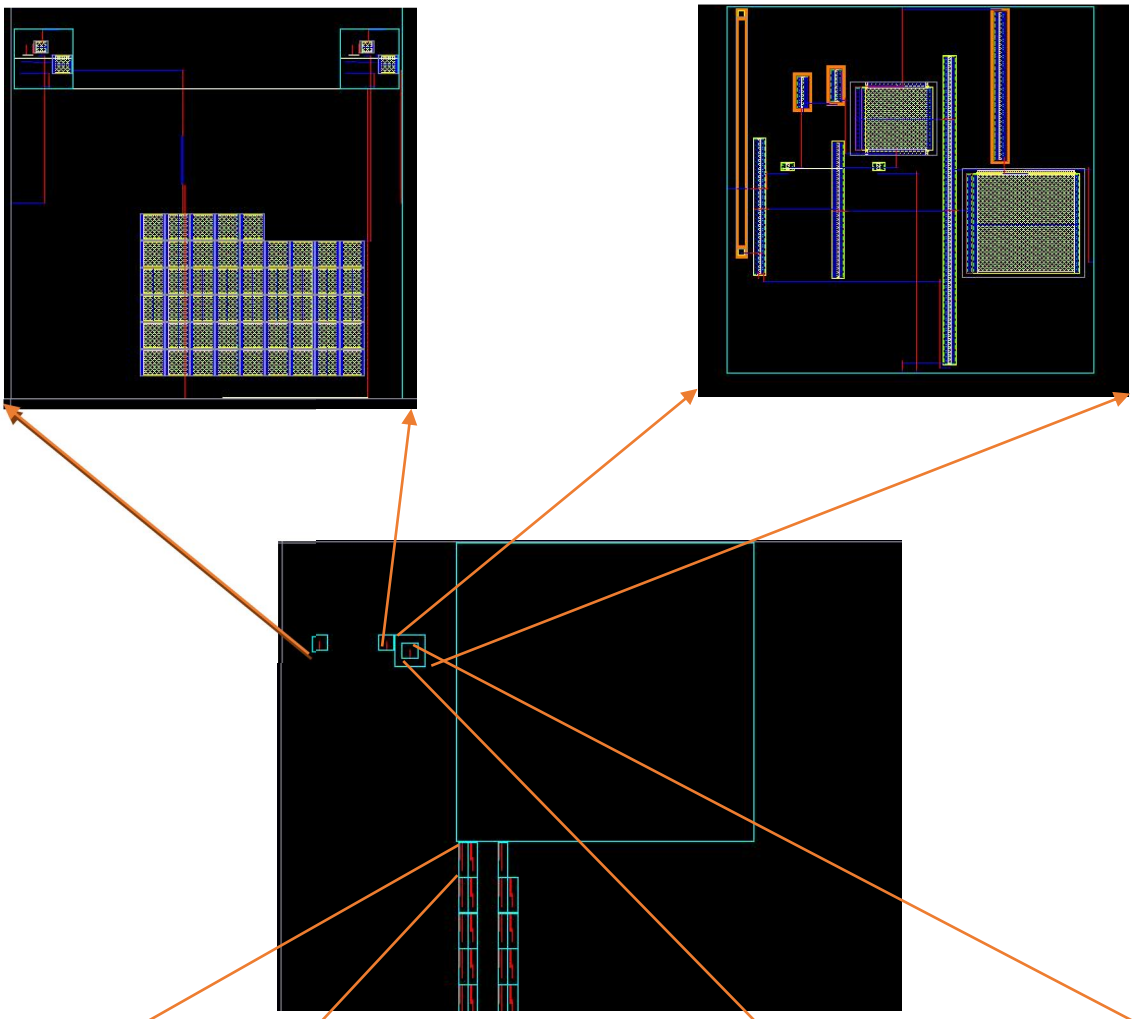
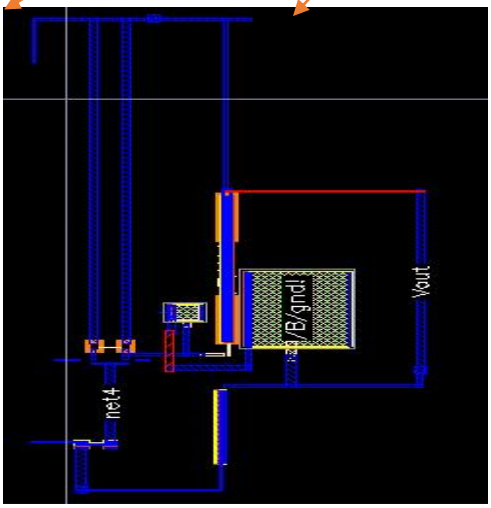
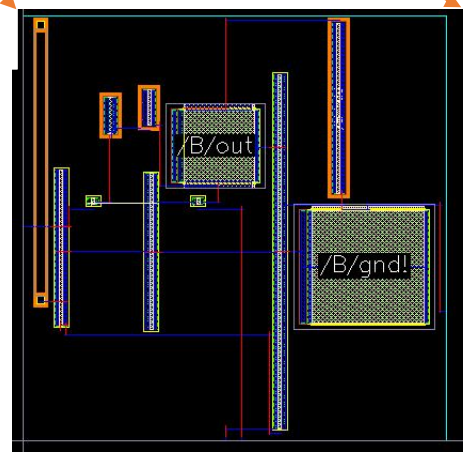


Figure. 5.8 Final Layout of Analog ASIC Design



Layout of CMOS Comparator



Layout of CMOS Op-Amp

References

[1] G.V Angelov, D.P Nikolakov, I.N Ruskova, E.E Gieva, M.L. Spasova, "Healthcare Sensing and Monitoring; Enhanced Living Environments"; Springer: Berlin/Heidelberg, Germany, 2019; pp. 226–262.

[2] J. Gao, Y. Yang, P. Lin, D.S. Park, "Computer vision in healthcare applications". J. Healthc. Eng. 2018, 2018, 5157020.

[3] A. Winter ,S. Stäubert , D. Ammon, "Smart medical information technology for healthcare". Methods Information 2018;57:e92–105. 10.3414/ME18-02-0004.

[4] Ji. Kwang Kim, Oh. Jung Hwan , G. B. Hwang, Oh. Seong Gwon, and Seung Eun Lee. "Design of Low-Power SoC for Wearable Healthcare Device".Journal of Circuits, Systems and Computers VOL. 29, NO. 06.

[5] HI. Zatrepalek, "FPGAs to solve tough DSP design challenges" 2012. p. 1–4.

[6] SA. Shufni, MY. Mashor, "ECG signals classification based on discrete wavelet transform, time domain and frequency domain features". Institute of Electrical and Electronics Engineers Inc.; 2015. p. 2.

[7] Xin. Liu,, Zheng, Yuanjin, Phyu, Myint Wai, "An Ultra-Low-Power ECG Acquisition and Monitoring ASIC System for WBAN Applications", IEEE Journal on Emerging & Selected Topics in Circuits & Systems, 2(1), 60 (2012)

[8] S. Lee, L. Yan, T. Roh, S. Hong, and H. J. Yoo, "A 75 μW real-time scalable body area network controller and a 25μW ExG sensor IC for compact sleep monitoring applications", IEEE J. Solid-State Circuits, 47(1), 323 (2012)

[9] P. Bonato, "Wearable sensors/systems and their impact on biomedical engineering", IEEE Eng. Med. Biol., 22(3), 18 (2003)

[10] Sanjeev Kumar Jain and Basabi Bhaumik, "An Ultra Low Power ECG Signal Processor Design For Cardiovascular Disease Detection", International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 857-860, 2015.

[11] L. Xie, L. Zheng, and G. Yang, "Hybrid Integration Technology for Wearable Sensor Systems," Internet Things Adv. Appl. Health., pp. 98–137, 2017

[12] G. Kanase and M. Nithin, "ASIC Design of a 32-bit Low Power RISC-V based System Core for Medical Applications". In 2021 6th International Conference on Communication and Electronics Systems (ICCES) (pp. 1-5). IEEE.

[13] S. Hesha, M. Shalan, M.W. El-Kharashi and M. Dessouky, "Digital ASIC Implementation of RISC-V: OpenLane and Commercial Approaches in Comparison". In 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) (pp. 498-502). IEEE.

[14] A. Birari, P. Birla, K. Varghese, and A. Bharadwaj, "A risc-v isa compatible processor ip". In 2020 24th International Symposium on VLSI Design and Test (VDAT) (pp. 1-6). IEEE.

[15] M. Gautschi, P.D. Schiavone, A. Traber, I. Loi, A. Pullini, D. Rossi, E. Flamand, F.K. Gürkaynak, and L. Benini, "Near-threshold RISC-V core with DSP extensions for scalable IoT endpoint devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems", 25(10), pp.2700-2713.

[16] A. Traber, F. Zaruba, S. Stucki, A. Pullini, G. Haugou, E. Flamand, F.K. Gurkaynak and L. Benini, "PULPino: A small single-core RISC-V SoC". In 3rd RISCV Workshop.

[17] K. Stoffelen, "Efficient cryptography on the RISC-V architecture". In International Conference on Cryptology and Information Security in Latin America (pp. 323-340). Springer, Cham.

[18] F. Farshchi, Q. Huang, and H. Yun, "Integrating NVIDIA deep learning accelerator (NVDLA) with RISC-V SoC on FireSim". In 2019 2nd Workshop on Energy Efficient Machine Learning and Cognitive Computing for Embedded Applications (EMC2) (pp. 21-25). IEEE.

[19] V. Herdt, D. Große, and R. Drechsler, “Closing the RISC-V compliance gap: Looking from the negative testing side”. In 2020 57th ACM/IEEE Design Automation Conference (DAC) (pp. 1-6). IEEE.

[20] A. Roelke, and M.R. Stan, “Risc5: Implementing the RISC-V ISA in gem5”. In First Workshop on Computer Architecture Research with RISC-V (CARRV) (Vol. 7, No. 17).

[21] A. Raveendran, V.B. Patil, D. Selvakumar and V. Desalphine, 2016, January. A risc-v instruction set processor-micro-architecture design and analysis. In 2016 International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI-SATA) (pp. 1-7). IEEE.

[22] Alan Hastings, The Art of Analog Layout. Upper Saddle River, NJ: Prentice-Hall, Inc., 2001

[23] Yamin Li, Tsinghua University Press, Computer Principles and Design in Verilog HDL, ISBN: 978-1-118-84109-9 June 2015

[24] J. Penders, M. Altini, C. V. Hoof and E. Dy, "Wearable sensors for healthier pregnancies", Proc. IEEE, vol. 103, no. 2, pp. 179-191, Feb. 2015

[25] P. Raj and A. C. Raman, The Internet of Things: Enabling Technologies, Platforms, and Use Cases. Taylor & Francis Group, 2017

[26] V. Misra, "Flexible technologies for self-powered wearable health and environmental sensing", Proc. IEEE, vol. 103, no. 4, pp. 665-681, Apr. 2015.

[27] A. Lymberis and A. Dittmar, "Advanced wearable health systems and applications-research and development efforts in the European union", IEEE Eng. Med. Biol. Mag., vol. 26, no. 3, pp. 29-33, May 2007

[28] J. P. Rojas, G. A. T. Sevilla, M. M. Hussain, Sci. Rep. 2013, 3, 2609; b) M. M. Hussain, A. M. Hussain, J. M. Nassar, A. T. Kutbee, A. Gumus, A. N. Hanna, presented at 2016 9th Int. Conf. Electrical and Computer Engineering (ICECE), Dhaka, Bangladesh December 2016

[29] M. Hussain, M. M. Hussain, Adv. Mater. 2015, 28, 4219; d) S. F. Shaikh, M. T. Ghoneim, G. A. T. Sevilla, J. M. Nassar, A. M. Hussain, M. M. Hussain, IEEE Trans. Electron Devices 2017, 64, 1894

[30] Behzad Razavi, “Design of Analog CMOS Integrated Circuits”