Design and Analysis of Distortion Reduction Techniques in Direct Conversion Receiver

Thesis

Submitted by

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Author's Declaration

This is to certify that

1. The thesis comprises my original work towards the degree of Doctor of Philosophy in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,
2. Due acknowledgment has been made in the text to all other material used.

Signature of Student

Certificate

This is to certify that the thesis work entitled "Design and Analysis of Distortion Reduction Techniques in Direct Conversion Receiver (DCR)" has been carried out by Milind Siddharthbhai Shah (201021003) for the degree of Doctor of Philosophy in Information and Communication Technology at this Institute under my supervision.

Thesis Supervisor

Prof. (Dr.)Sanjeev Gupta

Dedicated to

The Almighty

GOD SWAMINARAYAN

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Abstract

Direct-conversion is alternative wireless receiver architecture to the well-established super heterodyne architecture. Direct-conversion receiver (DCR) can offer highly integrated, low-power and low-cost hardware solutions for wireless/Cognitive Radio devices. However, direct conversion receivers are very sensitive to various RF impairments, which degrade its performance. This report present analysis and design of distortion reduction technique in direct conversion receiver (DCR). Such method enhances the overall performance of DCR by enhancing its immunity to various types of distortion.

Here modification in classical homodyne architecture is presented to make DCR more insensitive to distortion, with a stress put on minimum changes in the RF analog section with maximum ability of distortion removal. The proposed method gives liberty to the designer whether to incorporate in analog section or in the back-end Digital Signal Processing (DSP) section. Detailed investigation is carried out about the distortion reduction ability of proposed method. Theoretically, it is shown that proposed structure is able to reduce/remove (i) I/Q mismatch (ii) Even order distortions. Practically measured results also support theoretical claim. In addition, the results also show the ability of this method to reduce DC-offset distortion also. A simple but efficient method for calculation of optimized coefficients, which is able to remove distortion, is also presented. Theoretical results are first verified with analysis and later validated by experimental hardware setup. The results show the better performance of modified DCR architecture than conventional DCR architecture. With the proposed structure, a self-calibration procedure, without the need of extra hardware, can be implemented in direct conversion receiver to make it robust against distortions.

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List of Acronyms

AC	Alternating Current
ACRR	Adjacent Channel Rejection Ratio
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
AWGN	Additive White Gaussian Noise
BB	Base-Band
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CFO	Carrier Frequency Offset
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DC	Direct Current
DCR	Direct Conversion Receiver
DSB	Double Side-Band
DSP	Digital Signal Processing
DUT	Device Under Test
EDGE	Enhanced Data Rates for GSM Evolution
FDD	Frequency Division Duplex
FET	Field Effect Transistor
FM	Frequency Modulation
GSM	Global System for Mobile Communication
IC	Integrated Circuit
IF	Intermediate Frequency
IMD	Intermodulation Distortion
IMD2	Second Order Intermodulation Distortion
IMD3	Third Order Intermodulation Distortion
IIP2	Input-Referred Second Order Intercept Point
IIP3	Input-Referred Third Order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator

MDS	Minimum Detectable Signal
MOS	Metal Oxide Semiconductor
NF	Noise Figure
NMOS	N-Type Metal Oxide Semiconductor
PCB	Printed Circuit Board
PA	Power Amplifier
PM	Phase Modulation
PMOS	P-Type Metal Oxide Semiconductor
PSD	Power Spectrum Density
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Q	Quality Factor
SAW	Surface Acoustic Wave
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
SOC	System On-Chip
SSB	Single Side-Band
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TRX	Transmitter-Receiver, Transceiver
UMTS	Universal Mobile Telecommunication System
VCO	Voltage Controlled Oscillator
WCDMA	Wideband Code Division Multiple Access

Chapter 1

Introduction

1.1 Motivation

Wireless communication is assuming an undeniably huge part in regular day to day existence. Both settled and portable remote frameworks empower individuals and gadgets to exchange data without the requirement for wiring, which decreases execution expenses of communication systems and makes the use of wireless devices more convenient.

As wireless systems turn out to be increasingly well known, the interest for higher data rates, new services and functionality of wireless devices increases. In addition to fundamental communication abilities, present day wireless terminals join different extra innovations like digital camera, audio and video recorder and player and also different software applications like clock, calculator etc. With a specific end goal to implant these advances into wireless devices, factors like minimal cost, low power utilization and reduction

in dimensions of various blocks utilized for manufacturing of mobile devices become critical.

Because of recent advancements, there has been a developing pattern to decrease the quantity of parts involving the handset area of the wireless devices. Specifically, direct conversion architectures have increased expanding consideration due to their potential for a high level of integration and low power utilization [1-7]. Further, advances in semiconductor innovations, most eminently in CMOS technology, have made the way for the System On-Chip (SOC) design, in which radio and baseband modem and in addition application elements of a cell phone are embedded in a single chip.

The number of wireless standards has developed astoundingly, starting an enthusiasm for multi-standard and multi-band systems. To serve multiple systems, remote terminals should be reconfigurable. As the required adaptability is moderately simple to accomplish in the digital domain, research endeavors have centered in the later past on moving the analog to-digital conversion stage towards the antenna and performing more and more signal processing tasks, such as down-conversion, demodulation and distortion removal in digital domain. The multi-band operation requires evacuation of RF filtering as much as possible. This inclination is fortified by the pressure to reduce component count and board size.

Despite the fact that a huge advance has been made, the analog segment remains a bottleneck of the entire wireless system, particularly on the receiver side. As a result of reduced RF selectivity, solid blocking signals

might be available at the receiver input and cause its desensitization, impeding the reception of the desired signal. Despite of very small section of analog processing left, there is still place for analog imperfections, for example, crosstalk, nonlinearities creating inter-modulation and cross-modulation distortion, DC offset and gain/phase quadrature imbalances deteriorate the quality of the desired signal.

In direct conversion receiver (DCR), significant kinds of interferences are second-order Intermodulation distortion (IMD2), I/Q mismatch and DC offset. These distortions result from circuit nonlinearities combined with hardware layout asymmetries and unavoidable device parameter mismatches due to fabrication process variations. Because of random nature of device mismatches, the amount of distortion is itself random. Therefore, sufficient distortion rejection might not be guaranteed during the design stage.

Nevertheless, the receiver dynamic range must not degrade as a result of distortions. Accordingly, many methods of overcoming the problem have been proposed. Since the Low Noise Amplifier (LNA) and down-conversion mixer is the main contributor to distortions, most techniques focus on improving their performance by introducing certain post-production corrections. However, an issue of the sensitivity of these corrections to changes in the operating conditions becomes apparent.

The availability of DSP processing power in modern integrated receivers opens up new possibilities. Most importantly, the inherent lack of mismatches of digital circuits can be exploited in order to cancel imbalances in the analog

section and improve the distortion rejection. Moreover, cancellation of distortion can be carried out automatically, reducing production testing burden and allowing maintaining the improved performance over time.

Consequently, exploration of efficient on-chip distortion cancellation methods supported by digital signal processing is of interest. In conclusion, distortion removal method should not increase the component counts in the RF section of receiver, as well should not occupy large amount of resources in DSP back-end section. These stringent requirements can be fulfilled only by the computationally less complex method implemented fully in DSP back-end section. The method proposed in this thesis fulfills all this requirements.

1.2 Research Contribution

In the area of distortion removal methods, one innovative method has been proposed and implemented. The proposed method is based on a cascaded structure of multiplier and adder. A procedure to calculate multiplier coefficient also called as calibration constant for distortion removal is presented. A self calibration technique is also presented here. The Self calibration technique adapts calibration constants during the life of the system, rejects the distortion and regenerate the I/Q signals with minimum error. Multiplier and adder structure can be easily implemented in DSP back-end section. The self calibration technique does not require high computational complexity and therefore proposed method with self calibration technique can be easily implemented in DSP back-end section without requiring many

resources on DSP back-end. No hardware change in RF section of receiver is required to implement this method, as it is implemented in DSP back-end. This results into a cost-effective upgrading solution. In addition, there is no constraint regarding modulation scheme and power level in the proposed method. These features make the proposed method very attractive. The proposed distortion cancellation scheme is evaluated using advanced computer simulation tool. A corresponding hardware demonstrator has been designed and implemented..

1.3 Organization of the Thesis

The thesis is organized as follows. Chapter 2 introduces receiver design considerations. Various types of receiver architecture, their comparison, test parameters, working principle of direct conversion receiver and types of distortion in DCR are discussed. Particular stress is put on the origins of the distortions and factors affecting the distortions in DCR.

Chapter 3 provides an overview of methods that can be applied to improve reduction of distortions in DCR, including layout and circuit techniques as well as compensation and calibration schemes. Lastly, architectural methods are explored.

In chapter 4, a detailed mathematical analysis of proposed method is presented. The distortion removal ability of proposed method is also represented analytically.

Chapter 5 provides analysis and results for the proposed method. A hardware prototype is designed to evaluate the proposed scheme and measurement results of the proposed method are presented.

Conclusions of the research work carried out are presented in chapter 6. A brief performance comparison between the proposed method and other methods published in literature are also presented. At the end, suggestions for further work in the area of the distortion removal technique in DCR are also discussed.

Chapter 2

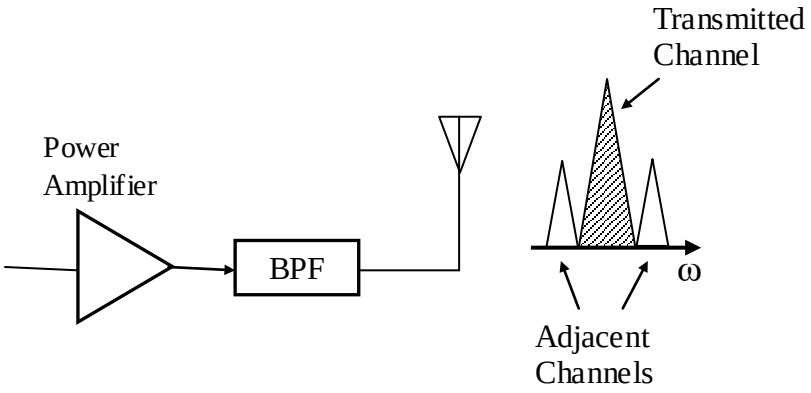
Receiver Design Considerations

2.1 General Considerations

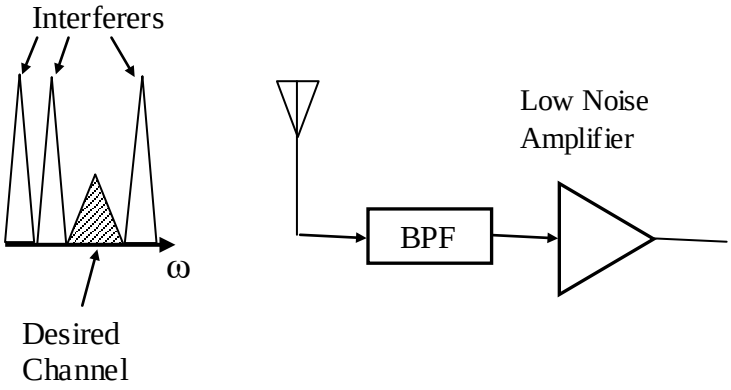
In wireless communication environment, the most important constraint is the limited spectrum allocated to each user. This constraint translates to a limited rate of information, mandating the use of sophisticated techniques and also impacts the design of the RF section. As shown in figure 2.1, the transmitter must employ narrowband modulation, amplification, and filtering to avoid leakage to adjacent channels and the receiver must be able to process the desired channel while sufficiently rejecting strong neighboring interferers [8].

In case of large in-band interferers accompany the received signal even after the front-end BPF, the nonlinearity of the following stages particularly that of the low-noise amplifier and the mixer, becomes important. These nonlinearities yield intermodulation products that fall in the desired channel.

These products not only distorting the amplitude, but also corrupt the zero-crossing points of the desired signal.



(a) *Transmitter with spectra of transmitted signal*



(b) *Receiver front end with spectra of received signal*

Figure 2.1 *Front end of a wireless transceiver*

Another important concern in the design of receivers is the dynamic range of the signals. With multipath fading and path loss, the required dynamic range for the received signal is typically 85 dB. As the minimum detectable signal is in the microvolt range, not only the input noise of the receiver but also cross-talk becomes critical in case of transceiver structure.

In recent generations of RF transceivers, the power amplifier is periodically turned ON and OFF to save power. However, the large current

drawn by the power amplifier introduces noise in the power supplies and may change the battery voltage by several hundred millivolts. For this reason, noise immunity and supply rejection become important.

Therefore, a receiver not only required to fight with external noise but also with the internal distortions. For effective removal of internal distortion, understanding the performance of receiver, in terms of noise and nonlinearities, is crucial. This chapter addresses the above topics. Apart from showing trends in receiver architectures, in particular, increase in their integration scale and the challenges associated with reduction of the system component count are highlighted.

2.2 Type of receiver architecture

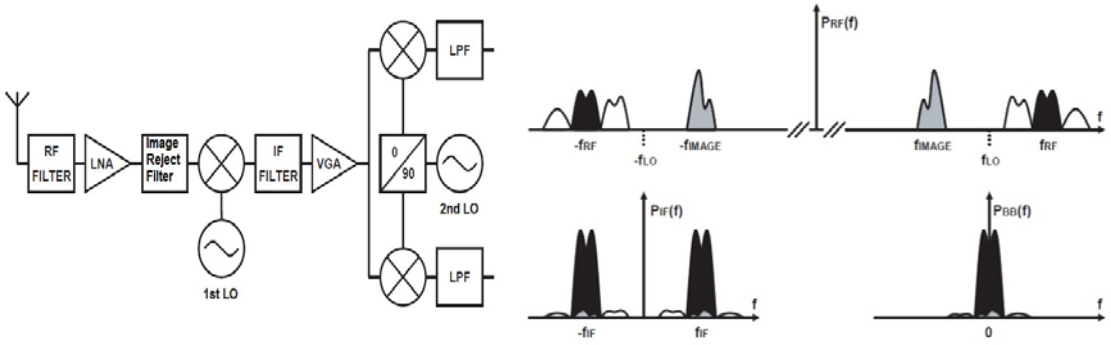
The main task of wireless receivers is detection of the incoming desired modulated signals. To achieve this goal, wireless receivers have to perform several functions, including tuning to the wanted signal carrier frequency, filtering out the undesired signals present at the receiver input and amplification of the wanted signal to compensate for power losses occurring during transmission.

In the receive path, preselect RF filters - either stand-alone or as part of duplexers - are used to suppress potentially large signals far outside of the desired channel. They are followed by a low noise amplifier, which increases the amplitude of weak received signals for further processing. Its name stems from the fact that as per Friis formula, its noise contribution has to be as

small as possible. RF signals are then translated down in frequency by mixers. After channel selection filtering, the transmitted information is recovered. Receiver architectures can be classified into two major groups: heterodyne and homodyne receivers. The names are derived from the Greek roots hetero for different, homo for the same and dyne for power. A distinguishing feature is the value of the LO frequency in relation to the RF frequency of the desired signal.

2.2.1 Heterodyne Receiver Architecture

The heterodyne receiver was for long time dominating receiver architecture in most wireless applications due to its superior selectivity and immunity to interfering signals.



(a) *Superheterodyne Receiver – Architecture* (b) *Superheterodyne Receiver – Spectra*

Figure 2.2 *Superheterodyne receiver*

A heterodyne receiver translates the desired input signal from the RF frequency to one or more preselected intermediate frequencies before demodulation. A block diagram of the superheterodyne receiver with one intermediate frequency is shown in figure 2.2(a). The channel selection is performed by means of an IF filter having a fixed transfer characteristic. After

additional amplification, the IF signal is shifted to baseband using a quadrature down-converter as shown in figure 2.2b [9]. The gain and phase quadrature mismatches are usually not important in this stage since the operating frequencies are low. Here, the desired channel is translated to much lower frequencies so as to relax the Q required of the channel-select filter. Therefore, selectivity and sensitivity of this receiver architecture is very high.

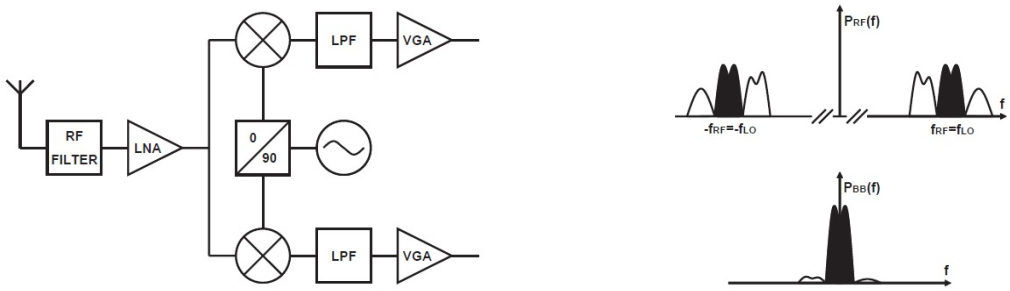
This architecture is suffering from a very serious problem called as Problem of Image. In a heterodyne architecture, the bands symmetrically located above and below the LO frequency are down-converted to the same center frequency. To avoid folding of interfering signals residing on the other side of the LO frequency to the common IF frequency, either a RF filter with sharp edges or a separate image-reject filter is required, which is shown in figure 2.2(a).

Despite its superior performance, the superheterodyne architecture is not suitable for monolithic integration because of presence of several expensive and bulky RF/IF filters. Since the IF filter has a fixed pass-band, optimized for a given wireless system, separate filters are necessary for multi-mode operation. This translates into large area and cost because many components are necessary and signal routing becomes complicated. An external image reject filter requires using a stand-alone LNA stage or additional pins for connecting output of an integrated LNA and input of an integrated RF mixer with the image reject filter. Extra pins are also required for connection to an IF filter [10].

2.2.2 Direct Conversion Receiver / Homodyne Receiver Architecture

Direct conversion receiver is also known as Homodyne receiver or Zero-IF receiver. The DCR was developed in 1932 by a team of British scientists searching for a design to surpass the superheterodyne. Not only did it have superior performance due to the single conversion stage, but it also had reduced circuit complexity and power consumption. The simplification of performing only a single frequency conversion reduces the basic circuit complexity but other issues arise, for instance, regarding dynamic range and various types of distortion. Despite of all these benefits due to technical challenges and non-availability of today's high level technology made this technique rather impractical around the time of its invention. Rapid development in VLSI technology regain the interest of various researchers in development and analysis of DCR[1-9].

A zero-IF receiver translates the desired RF signal directly to baseband for information recovery. Figure 2.3(a) shows its block diagram, while an example of signal spectra before and after demodulation is shown in figure 2.3(b) [11]. The quadrature down-converter performs the same function as the last stage of the superheterodyne receiver [figure 2.2(a)], but it usually operates at substantially higher frequencies. The channel selection is done with low-pass filters, which are much easier to integrate than band-pass filters.



(a) *Direct conversion receiver architecture* (b) *Direct conversion receiver spectra*

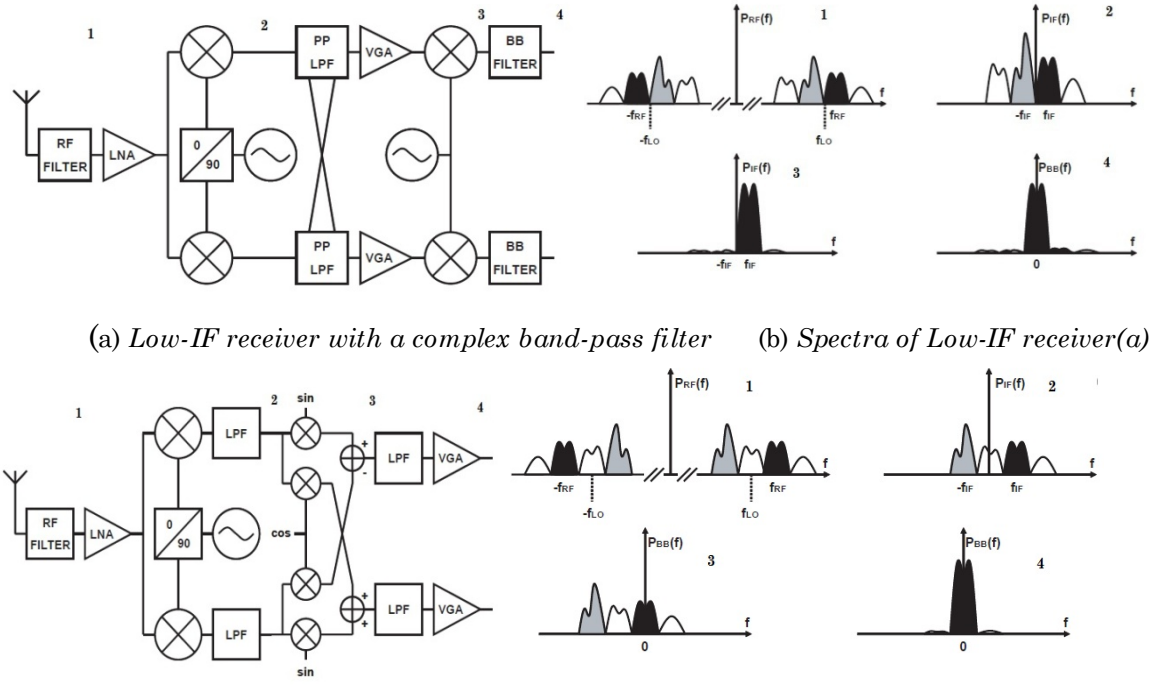
Figure 2.3 *Direct Conversion Receiver*

The conceptually simple homodyne architecture presents a number of challenges, like gain and phase quadrature mismatches, undesired low-frequency distortion and DC-offsets.

2.2.3 Low-IF Receiver Architecture

To reduce the impact of both low-frequency distortion and DC-offsets, low-IF receiver architecture can be employed [12-13]. It can be viewed as a special case of the homodyne architecture. No image reject filters are needed so the low-IF architecture has the same benefits in terms of reduced component count as the standard homodyne architecture.

Channel selection in low-IF receivers can be performed in two ways. In the first method, the mirror signal is first suppressed by means of complex pass-band filters, centered around the IF frequency, as shown in figure 2.4(a).



(a) *Low-IF receiver with a complex band-pass filter* (b) *Spectra of Low-IF receiver(a)*

(c) *Low-IF receiver with a real baseband filter* (d) *Spectra of Low-IF receiver(c)*

Figure 2.4 *Low-IF receiver*

Such filters can be easily built from baseband prototypes using a poly-phase filtering technique. After suppression of the mirror signal, the final downconversion can be performed by multiplication with a sine, which is usually carried out in the digital domain [figure 2.4(b)]. The second downconversion stage does not require quadrature LO signals.

Alternatively, a real baseband filter can be used to filter out all but adjacent channels [figure 2.4(c)]. Next, a sophisticated quadrature mixing is carried out with four multipliers, an adder and a subtractor, which effectively calculates a real part of a product of two complex signals. Using this technique, spectrum of the complex IF signal is moved in one direction only, as shown in figure 2.4(d). Final channel filtering is performed at baseband using

real low-pass filters. The same technique has been applied in a so-called wideband-IF receiver [14].

The advantage of low-IF receivers in comparison to zero-IF receivers is that there is no DC-offset problem as it can be removed before the desired signal is shifted to DC. Low-frequency distortion is also attenuated.

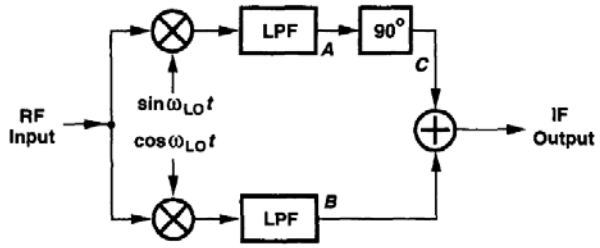
The main challenge in a practical application of the low-IF receiver topology is the performance of image signal suppression, which can be insufficient due to I/Q imbalances. Additionally, if the channel selection is performed in the digital domain, high-performance analog-to-digital converters are needed to resolve a weak desired signal with sufficient number of bits while digitizing a strong mirror signal at the same time.

2.2.4 Image-Reject Receiver

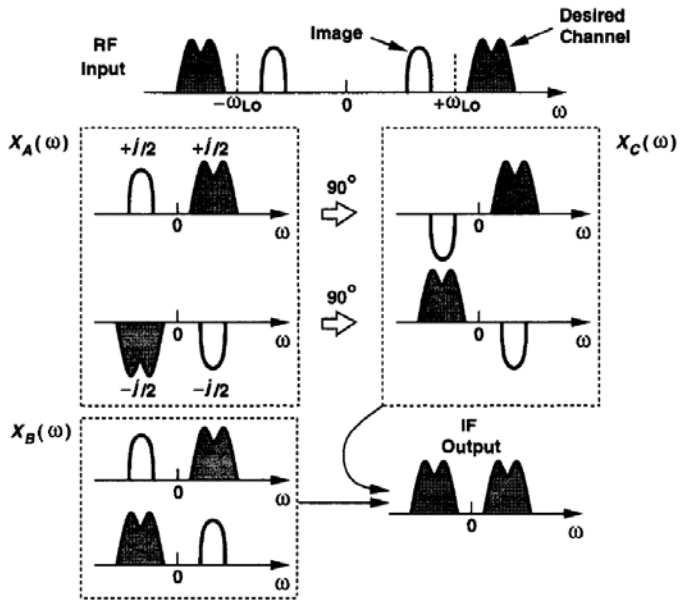
Enforced by the trends to reduce the cost and size of the RF front-end, alternative heterodyne architectures have been proposed. The trade-offs governing the use of image-reject filters in heterodyne architectures have motivated RF designers to seek other techniques of suppressing the image. Image reject filters can be removed by employing image reject receivers based on Hartley or Weaver architecture but at the expense of additional power consumption [15].

(1) Hartley Architecture

An image-reject architecture originating from a single-sideband (SSB) modulator introduced by Hartley [16] is illustrated in figure 2.5. Hartley's circuit, mixes the RF input with the quadrature phases of the local oscillator, low-pass filters the resulting signals, and shifts one by 90° before adding them together.



(a) *Heartly Architecture*



(b) *Graphical Analysis of Heartly Architecture*

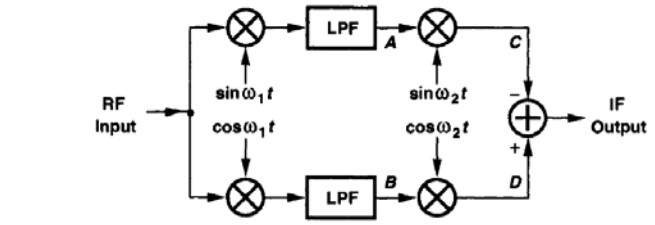
Figure 2.5 *Heartly Image Reject Architecture*

A critical issue in the Hartley architecture is the gain mismatch resulting from the 90° phase shift operation. In addition other matching requirements in this topology are still much more stringent than those in

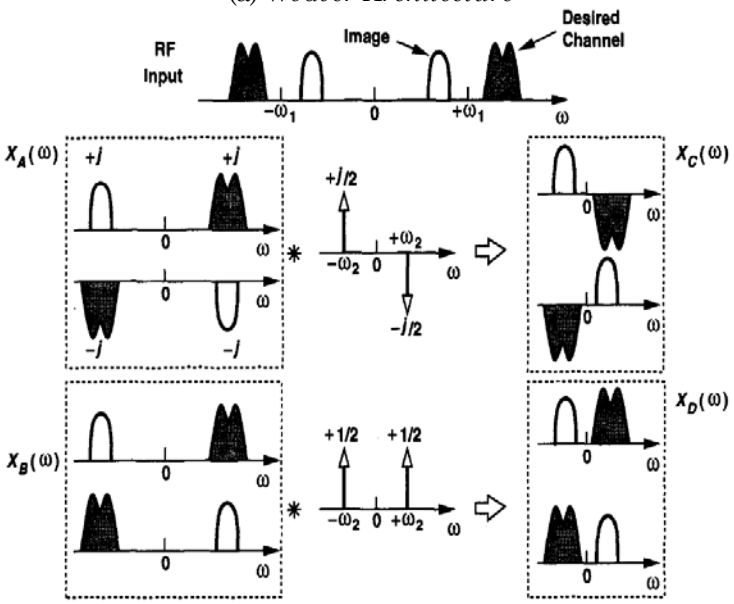
homodyne receivers. Monolithic implementation of the Hartley architecture entails other issues as well. Detailed analysis is presented in [4].

(2) Weaver Architecture

In heartly architecture, critical problem is to achieve 90^0 phase shift over entire channel bandwidth. This problem is solved in weaver architecture by shifting carrier signal by 90^0 phase shift. In the Hartley architecture, we noted that quadrature downconversion followed by a 90° phase shift produces in the two paths the same polarities for the desired signal and opposite polarities for the image. Illustrated in figure 2.6, the Weaver architecture [17] replaces the 90° stage by a second quadrature mixing operation to perform essentially the same function.



(a) *Weaver Architecture*



(b) *Graphical Analysis of Weaver Architecture*

Figure 2.6 *Weaver Image Reject Architecture*

Numerous papers showing implementations of a direct conversion concept for cellular applications exist, clearly confirming the widespread interest in the homodyne architecture. Direct conversion receivers for the GSM system are documented in [18-22]. Receiver implementations based on a direct conversion architecture for CDMA applications are shown in [23-24], while direct conversion receivers for WCDMA UMTS are presented in [25-32]. Direct conversion architecture is also preferable for multi-mode solutions. Examples of dual-mode GSM-WCDMA receivers can be found in [33-35]. Due to entirely different system requirements of GSM and WCDMA standards, a low-IF topology is often preferred for GSM while a normal homodyne architecture is used for WCDMA.

Thus DCR is choice of the today's designer due to low component count. But distortions affect its performance. To eliminate the effect of distortions, sources of distortions should be investigated in detail. In next section, distortions in direct conversion receiver are described in detail.

2.3 Distortions in Direct conversion receiver

Direct translation of the spectrum to zero frequency entails a number of issues that do not exist or are not as serious in a heterodyne receiver. These distortions are described below:

2.3.1 DC Offsets

Since in a direct conversion receiver the down-converted band extends to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages. To understand the origin and impact of offsets, consider the receiver shown in figure 2.7 [36], where the LPF is followed by an amplifier and an A/D converter.

(a) *Self-mixing of LO signal* (b) *Self-mixing of a strong interferer*

Figure 2.7 *DC-offset generation due to Self-mixing*

The isolation between the LO port and the inputs of the mixer and the LNA is not infinite; that is, a finite amount of feed through exists from the LO port to points A and B [figure 2.7(a)]. Called "LO leakage," this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, bond wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the LO signal, thus producing a DC component at point C. This phenomenon is called "self-mixing." A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself [figure 2.7(b)].

The problem of offset is exacerbated if self-mixing varies with time. This occurs when the LO signal leaks to the antenna and is radiated and

subsequently reflected from moving objects back to the receiver. For example, when a car moves at a high speed, the reflections may change rapidly. Under these conditions, it may be difficult to distinguish the time-varying offset from the actual signal.

We should also note that the problem of offset is much less severe in heterodyne architectures. Since the first LO frequency is not equal to the input carrier frequency, self-mixing may arise only for interferers [figure 2.7(b)], and DC offsets thus generated can be removed because the IF signal is far from zero frequency. Furthermore, in analog FM systems the second IF is nonzero and in digital modulation systems signal amplification and (partial) channel filtering at the first IF simplify the removal of the offset after the second downconversion.

2.3.2 I/Q Mismatch

Direct conversion receiver incorporates quadrature mixing. This requires shifting either the RF signal or the LO output by 90°. Shifting the RF signal generally entails severe noise-power-gain trade-offs, making it more desirable to use the topology in which LO signal is shifted 90°. In either case, the errors in the nominally 90° phase shift, and mismatches between the amplitudes of the I and Q signals corrupt the down-converted signal constellation, thereby raising the bit error rate. Note that, as shown in figure 2.8, all sections in the I and Q paths contribute gain and phase error.

Figure-2.9 shows the resulting signal constellation. This effect can be better seen by examining the down-converted QPSK signals in the time domain [figure 2.10]. Gain error simply appears as a non-unity scale factor in the amplitude. Phase imbalance, on the other hand, corrupts each channel by a fraction of the data pulses in the other channel; in essence degrading the signal-to-noise ratio if the I and Q data streams are uncorrelated.

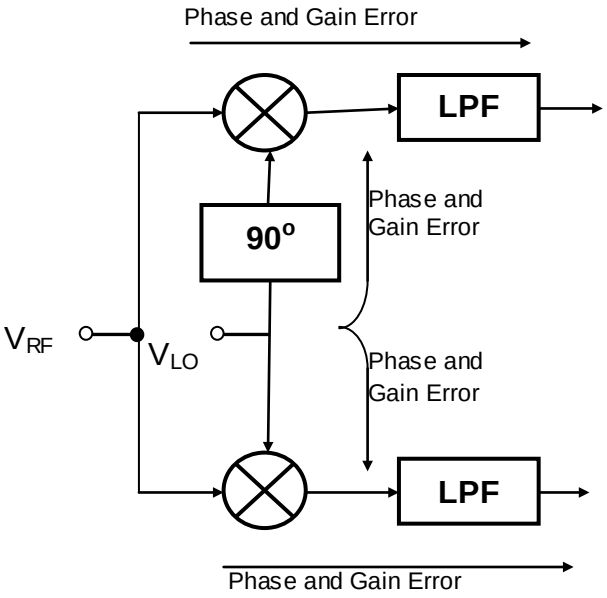
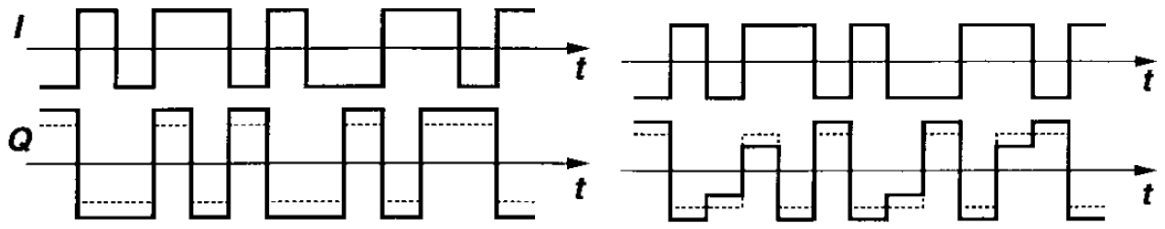


Figure 2.8 *I/Q mismatch contributions by various stages*

(a) *Gain error* (b) *Phase error*

Figure 2.9 *Effect of I/Q mismatch on QPSK signal constellation*



(a) *Gain error* (b) *Phase error*

Figure 2.10 *Effect of I/Q mismatch on a demodulated QPSK waveform*

While heterodyne receiver may also employ l/Q downconversion in the last stage, their mismatch requirements are much more relaxed. This is for two reasons. First, since the frequency at which I and Q phases are separated is about one to two orders of magnitude lower than that in homodyne counterparts, the two paths are much less sensitive to mismatches in parasitics. Also, in IC design, the lower frequency allows the use of large devices to improve the matching without excessive power dissipation. Second, in heterodyne receivers, the signal is amplified by approximately 50 to 60 dB before l/Q separation, requiring only one or two more stages afterwards. By contrast, each channel of a DCR incorporates several stages of gain and filtering, each of which contributes mismatches. We should also note that heterodyne receiver can perform the l/Q separation in the digital domain to avoid mismatch issues whereas DCR cannot. The problem of l/Q mismatch has been an obstacle in discrete implementations, but it tends to improve as monolithic integration embraces more sections of DCR. Furthermore, since mismatches vary negligibly with time, signal processing techniques may be utilized to correct the points in the constellation.

2.3.3 Even-Order Distortion

Even-order nonlinearity is an important RF imperfection in all wireless receivers. In heterodyne receivers, it manifests itself through half-IF spurious responses. Careful frequency planning, including proper selection of the IF frequency, is required to protect the receiver from such distortion. In DCR, even-order nonlinearity is responsible for low-frequency even-order intermodulation distortion, which effectively increases the noise floor of the direct conversion receiver.

Suppose, as illustrated in figure 2.11, two strong interferers close to the channel of interest experience a nonlinearity such as $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ in the LNA [6]. If $x(t) = A_1 \cos\omega_1(t) + A_2 \cos\omega_2(t)$ then y(t) contains a term, $\alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$, indicating that two high-frequency interferers generate a low-frequency beat in the presence of even-order distortion. Upon multiplication by $\cos\omega_{LO}t$ in an ideal mixer, such a term is translated to high frequencies and hence becomes unimportant. In reality, however, mixers exhibit a finite direct feed through from the RF input to the IF output. This is because, mixers typically suffer from some asymmetry and their operation can be viewed as $v_{RF}(t)(a + A\cos\omega_{LO}t)$, where a is a constant. Thus, a fraction of $v_{RF}(t)$ appears at the output with no frequency translation. In typical differential mixers, the beat signal is attenuated by only 30 to 40 dB as it couples to the output.

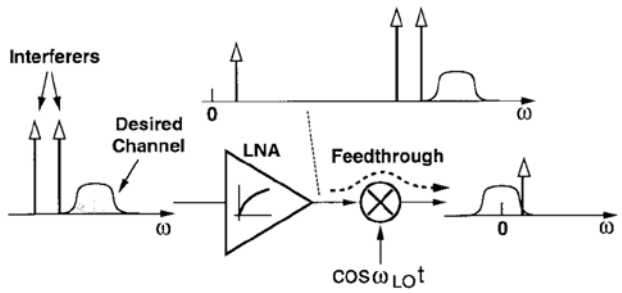


Figure 2.11 *Effect of even-order distortion on interferers*

Such distortion can be reduced by sufficient filtering of interferers before they reach the nonlinear components of the RF front end. However, highly selective RF filtering is not welcome in modern transceivers. In many practical wireless receivers, downconversion mixers are main contributors to even order distortion as shown in figure 2.12[10]. This is due to the fact that low-frequency even-order distortion products generated in the LNA are normally filtered out by AC coupling or band-pass filtering between the LNA and the downconversion mixer.

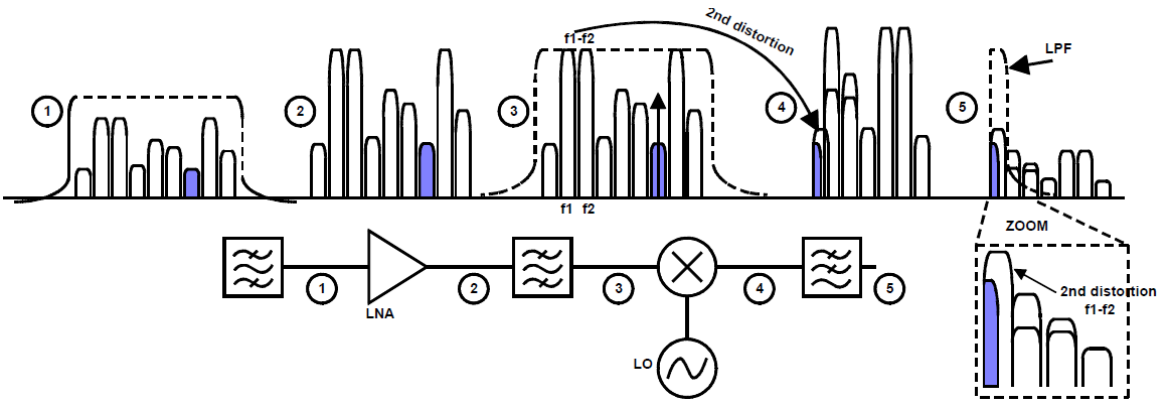


Figure 2.12 *Spectral aliasing in DCR due to even-order intermodulation distortion*

Sufficient filtering of interferers before the active part of the receiver RF front end is required. However, this approach lies in contradiction to the

current trends aimed at reduction of the component count of mobile transceivers. In particular, certain RF filtering stages like interstage surface-acoustic wave filters in CDMA receivers are not welcome, not only because of their size and cost but also because they degrade receiver sensitivity by introducing in-band loss. Furthermore, tunable band-pass RF filters are preferred in multi-band transceivers instead of a bank of fixed band RF filters, as they occupy less space. Since tunable filters usually have poorer attenuation in their stop bands, they provide less attenuation of out-of-band interferers. Therefore, second order intermodulation distortion is a serious issue in modern receiver design and techniques of its mitigation have to be provided to fulfill system requirements.

2.3.4 Flicker Noise

Since the down-converted spectrum extends to zero frequency, the 1/ f noise of devices substantially corrupts the signal, a severe problem in MOS implementations. For this reason, it is desirable to achieve a relatively high gain in the RF range, for example, through the use of active mixers rather than passive mixers. The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate at relatively low frequencies, they can incorporate very large devices to minimize the magnitude of the flicker noise [36]. In addition, if DC free coding is employed, the down-converted signal and hence the noise can be high-pass filtered.

2.3.5 LO Leakage

In addition to introducing DC offsets, leakage of the LO signal to the antenna and radiation there from creates interference in the band of other receivers using the same wireless standard [4]. The design of the wireless standard and the regulations of the Federal Communications Commission (FCC) impose upper bounds on the amount of in-band LO radiation, typically between -50 dBm and -80 dBm.

Chapter 3

Distortions Reduction Techniques in Direct Conversion Receiver

3.1 General Considerations

Direct conversion receiver architecture is very attractive because of its simplicity and amiability to monolithic integration. But, as discussed in the previous section, it suffers from various distortions such as dc-offset, even-order distortion and I/Q mismatch problem. Efforts have been made to analyze various sources of distortion and various distortion reduction/removal techniques suitable for integrated RFIC receiver suggested by various researchers. Brief description with their strengths and weaknesses of various distortion cancellation or removal techniques are mentioned here.

3.2 DC-Offset Reduction Techniques

In the DCR, the desired signal is down-converted directly to a baseband, and the offset signals generated by the self-mixing problem can corrupt the baseband desired signal, as shown in figure 2.5. Therefore, it is necessary to mitigate these offset signals in order to successfully demodulate the desired signal at the DCR. The offset signals generated by the self-mixing problems can be classified into two types.

One is the DC offset generated by local oscillator (LO) leakages, and the other is the self-mixed interference generated by interference leakages [6]. The DC offset is a time-invariant offset signal while the self-mixed interference is a time varying offset signal. Numerous methods are proposed in literature to solve this problem. These methods can be classified in following categories:

3.2.1 AC-coupling

This is a simple approach to employ high-pass filtering in the down converted signal path to remove DC component present due to self-mixing. But this technique corrupt the down converted baseband signal if it exhibits a peak at DC, such as M-ary random data. In addition to cover full baseband, high pass filter must have the corner frequency of less than 0.1% of the data rate. For low data rate application, this frequency becomes so low that the high-pass filter implementation required large capacitors and resistors, which is not desirable. A low corner frequency in the high pass filter may also lead to temporary loss of data in the presence of wrong initial conditions [9]. If no data

is received for a relatively long time, the output DC voltage of the high pass filter (HPF) droops to zero. Now if data is applied, the time constant of the filter causes the first several bits to be greatly offset with respect to the detector threshold, thereby introducing errors. A possible solution to the above problems is to minimize the signal energy near DC by choosing "DC-free" modulation schemes. One possible solution to this problem is to select "DC-free" modulation schemes, such as binary frequency shift keying (BFSK) [5].

3.2.2 DC-Offset cancellation

In offset cancellation method, wireless device store the dc-offset on a capacitor during ideal mode and this stored offset will be subtracted from the received signal during active mode. In wireless standards that incorporate time-division multiple access (TDMA), each mobile station periodically enters an idle mode so as to allow other users to communicate with the base station. The offset in the receive path can be stored on a capacitor during this mode and subtracted from the signal during actual reception. Figure 3.1[6] shows a simple example, where capacitor stores the offset between consecutive TDMA bursts while introducing a virtually zero corner frequency during the reception of data.

For typical TDMA frame rate, offset cancellation is performed frequently enough to compensate variations due to moving objects. The major issue in the circuit of figure 3.1 is the thermal noise of S_1 (kT/C noise).

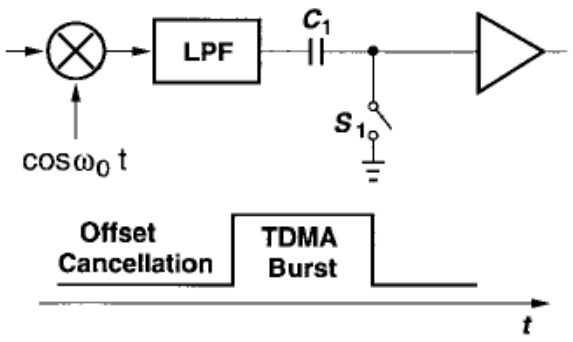


Figure 3.1 *Offset cancellation in a TDMA system*

For example, if a 1μVrms signal received at the antenna experiences a gain of 30dB before offset cancellation, then C_1 must be at least 200 pF so that kT/C remains 15 dB below the signal level. If the signal path is differential, then two capacitors, each equal to 400 pF, are required so that the overall noise is still 15 dB below the signal. Thus, with I and Q channels, the total capacitance reaches 1.6 nF. Note that since C_1 is a floating capacitor, it cannot be easily implemented with MOS transistors. Structures providing so much capacitance typically occupy a very large area.

A general difficulty with offset cancellation in a receiver is that interferers may be stored along with offsets. This occurs because reflections of the LO signal from nearby objects must be included in offset cancellation and hence the antenna cannot be disconnected (or "shorted") during this period. While the timing of the actual signal (the TDMA burst) is well-defined, interferers can appear any time. A possible approach to alleviating this issue is to sample the offset (and the interferer) several times and average the results.

3.2.3 Adaptive DC-Offset cancellation

In adaptive methods, amount of dc-offset is estimated with the help of various techniques and then this estimated dc-offset is subtracted from the received signal. Such methods are discussed in [18,37-41]. They can be effective in mitigating time-invariant offsets while they cannot effectively mitigate time-varying offsets. Some digital signal processing methods for mitigating the time-varying offset have been introduced in [42]. However, the cancellation methods in [42] cancel the time-varying offsets only when the time-varying offsets are periodic. A novel receiver structure based on the adaptive interference cancellation (IC) method as shown in figure 3.2 is suggested in [43].

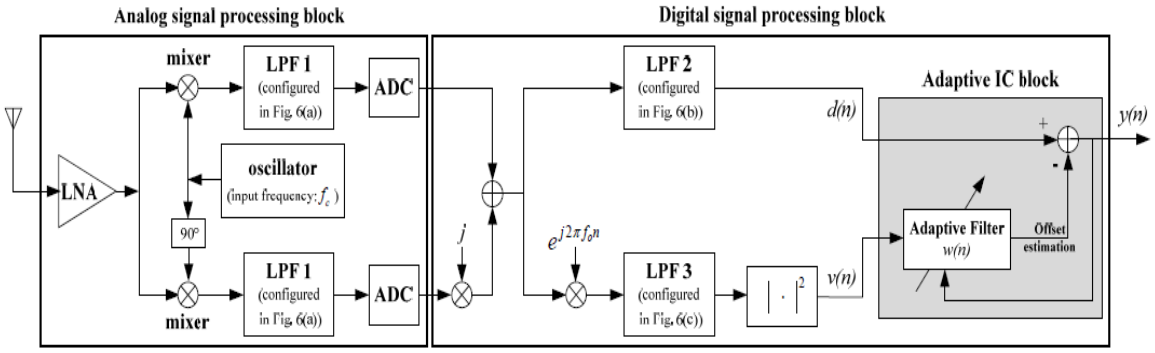


Figure 3.2 R*eceiver structure based on self-mixed interference cancellation procedure*

As all the techniques are implemented mainly in DSP section, increase in the component count in RF section is not an issue, but they do not take care of other distortions. This may result into the requirement of other methods to

deal with remaining distortions, results in the increase in component count and computational load.

3.3 Even-order distortion reduction techniques

In direct conversion receiver, second order intermodulation distortion (IMD2) is a significant kind of interference because it falls in the baseband occupied by a down converted baseband signal. A large number of techniques have been suggested by various researchers. Brief description with their strengths and weaknesses of various IMD2 cancellation or removal techniques are mentioned here.

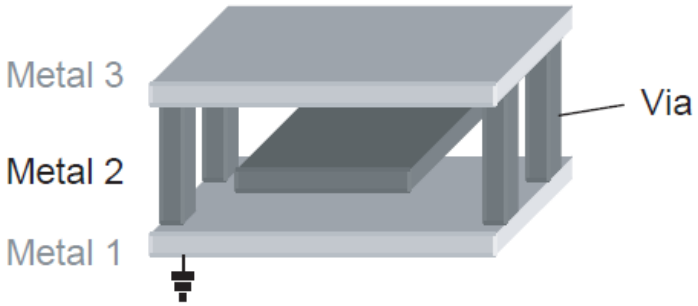
3.3.1 Layout Techniques

Layout techniques can be classified into device-matching improvement techniques and RF-LO coupling reduction techniques.

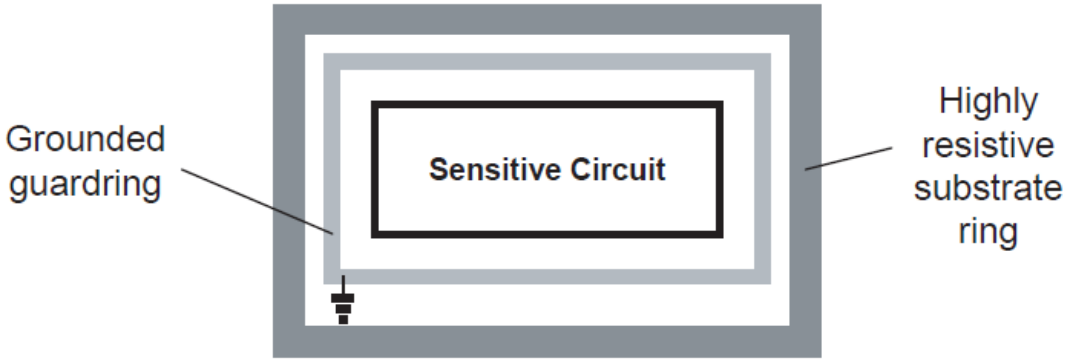
Careful, symmetrical layout of both active and passive devices as well as their interconnects improves matching between differential paths of the circuit. Parameter mismatches of active devices are significantly reduced by applying a so-called common centroid layout technique, which includes cross-coupling and inter-digitation patterns.

Another category of IMD2-cancelling layout techniques deals with minimization of the impact of RF self-mixing on the overall even order distortion performance. Three coupling mechanisms responsible for self-

mixing phenomenon need attention: EM crosstalk, substrate coupling as well as ground and power supply bounce. Shielding of LO transmission lines by using neighboring grounded metal layers [figure 3.3(a)] reduces EM crosstalk since metal ground planes confine electromagnetic fields [44].



(a) *Shielding of LO transmission lines*



(b) *Substrate coupling suppression*

Figure 3.3 *LO-RF coupling reduction techniques*

The disadvantage is an increased power consumption of LO buffers driving such transmission lines required to maintain high-quality LO waveforms. Substrate coupling can be suppressed by placing highly resistive substrate rings around the sensitive downconversion mixer circuit [figure 3.3(b)]. Other substrate coupling reduction techniques are reported in [45].

Finally, ground and power bounce can be reduced by connecting circuit and substrate grounds together using densely placed substrate contacts as well as by using de-coupling capacitors between power and ground lines.

All of the presented layout techniques increase IIP2 on average i.e. shifts its histogram toward higher values. However, they cannot totally remove circuit and interconnection asymmetries as well as completely eliminate random parameter variations.

3.3.2 Circuit Architecture for Even-order distortion removal

Circuit techniques focus on decreasing second order nonlinearity of mixer devices rather than on reducing mismatches between them. Various categories of circuit techniques are as below.

(a) RC Degenerated Input Stage

In MOS transistor, negative feedback can be applied by connecting an impedance between the source of the active device and ground. In case of simple resistive feedback, this technique reduces the effective first and higher-order transconductances of the transistor at all frequencies. Since only second-order transconductance has to be reduced, it is advantageous to apply negative feedback with resistor and capacitor connected in parallel, as shown in figure 3.5 [45]. At low frequencies, the absolute value of the impedance of such network is determined mainly by the resistance R, implying a strong negative feedback and significant attenuation of low-frequency distortion products. At

high frequencies, the absolute value of the impedance is determined by the capacitance C, which shorts R to ground so that effectively no feedback exists. Consequently, the effective transconductance is larger, which improves mixer noise performance.

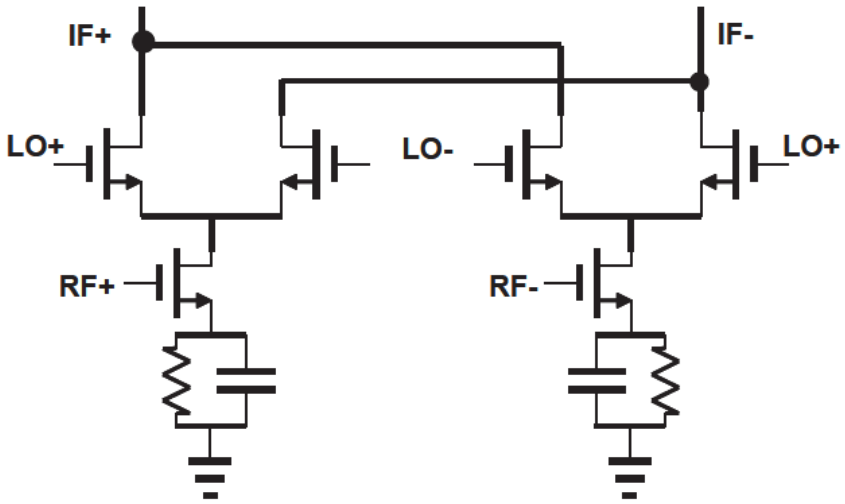


Figure 3.4 *IMD2 cancellation with RC degenerated input stage*

Advantage of this method is easy implementation. But the drawbacks are (i) Resistor will occupy larger area on chip, (ii) This negative feedback attenuate desired signal also (iii) This method does not alleviate the problem of second order distortion of the complete mixer because of the remaining distortion products due to RF-LO coupling.

(b) Input Stage with IMD2-Cancelling Biasing Circuit

Second order intermodulation distortion generated in the mixer input stage can be also reduced by using a special kind of biasing configuration. This biasing method is introduced in [46] and patented in [47], the biasing arrangement is shown in figure 3.5.

Advantage of this method is that, it is more suitable for mixers operating at low supply voltage since there are no linearizing feedback components, which consume voltage headroom. But drawback is inability to cope with coupling mechanisms and distortion generated by the switching stage.

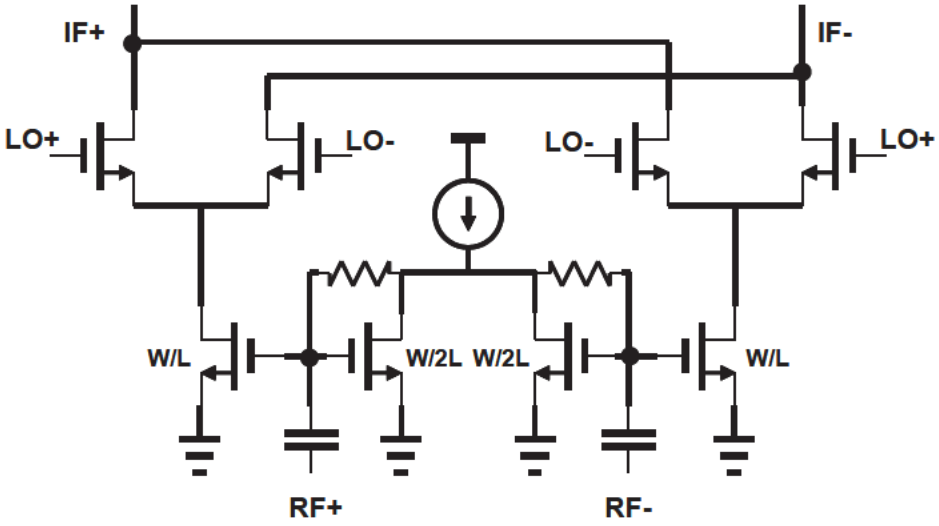


Figure 3.5 *Mixer core with IMD2-cancelling biasing circuit*

(c) Reduction of Common Mode Distortion with CMFB

IMD2 can be reduced by exploiting common mode feedback loops in order to eliminate the flow of common mode distortion current through certain elements, which could otherwise convert it to differential mode. Two such methods have been proposed.

The first technique suppresses common mode IMD2 current flowing through the mixer load impedances by injecting almost equal amplitude but out-of-phase common mode distortion current to the outputs of the switching stage, as shown in figure 3.6 [48-49]. In this manner, load impedance

mismatches contribute negligibly to the effective mixer mismatch. The amount of injected current is determined by the CMFB loop gain. Mismatches between the current sources affect the performance of this technique. Since only low-frequency distortion has to be suppressed in downconversion applications, relatively large (and thus better matching) current sources can be used so in practice performance degradation is small.

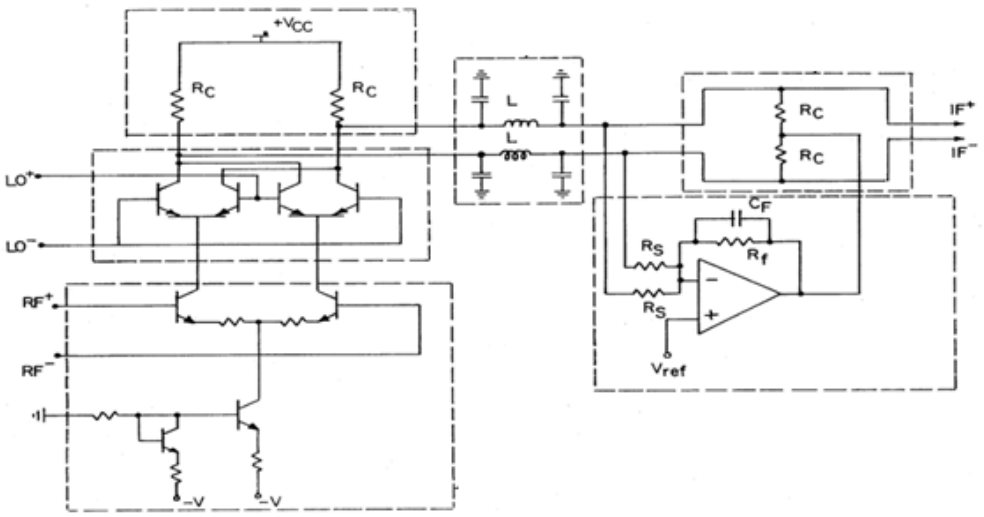


Figure 3.6 *Distortion cancellation with common mode feedback loop*

This method has advantage that it reduces the common mode distortion. But drawback is that in low voltage CMOS mixers, it does not solve all mismatch problems.

The second technique eliminates flow of common mode IMD2 current through the switching stage of the mixer by either controlling the biasing current of the mixer input stage [50] or by injecting common mode distortion current to the outputs of the input stage [51]. In both cases, the amount of current is controlled by the common mode feedback loop, which senses

common mode distortion voltage at the output of the mixer. This method effectively eliminates mismatch terms associated with switching stage leakage mechanisms and output stage imbalances. However, RF-LO coupling mechanisms and switching stage nonlinearities are not addressed.

(d) Other Techniques

In addition to the techniques described above, several other IMD2 mitigation methods based on certain circuit configurations have been published. Since they are less general in nature than the previous techniques, only a brief description is provided below.

In [52], a method for reducing even order distortion based on injection of out-of-phase distortion current has been presented. It is suitable only for mixers implemented in bipolar technologies. The idea is to utilize an additional bipolar differential pair. The bases of transistors forming the differential pair are connected to the outputs of the mixer and inject out-of-phase even-order distortion current, reducing the flow of distortion current through the load resistors. Good suppression of distortion is achieved provided that additional transistors are appropriately scaled to produce the amount of distortion close to that generated in the mixer core. Process variations as well as varying operating conditions limit the effectiveness of this technique.

Even-order distortion caused by RF-LO crosstalk can be significantly reduced by using harmonic mixers. In such mixers, the RF input signal is mixed with one of the higher order LO harmonics, usually the second

harmonic. The impact of the fundamental LO harmonic coupling on second-order distortion mechanisms becomes much smaller. However, second-order distortion products due to active device nonlinearities and mismatches still exist. Moreover, harmonic mixers offer smaller conversion gain for a given current consumption than traditional mixers.

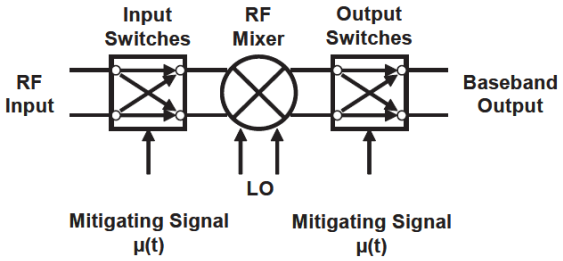
An interesting concept, which reduces the impact of indirect leakage and distortion generated by the switching stage due to parasitic capacitances loading the switching pairs, has been presented in [53] and [54]. The idea is to attach an inductor to the common source node of the switches so as to cause a parallel resonance with the parasitic capacitor at the LO frequency. The effective impedance loading the common source node of the switching pair is thus high, which decreases the indirect leakage and linearizes the switching devices via negative feedback. Consequently, they contribute less to the effective mixer mismatch. However, the mismatch coefficients associated with coupling and output stage mismatches remain unaffected by the proposed technique.

Apart from its inability to deal with RF-LO coupling, the concept of tuning out parasitic capacitances by means of integrated inductors entails several practical limitations. First, such solution can function only for mixers operating in a single band. In case of multiband transceivers, this would require having separate mixers for each band, which increases the total chip area. As inductors are usually used in low-noise amplifiers and oscillators, adding another set of these passive devices to the whole receiver would make

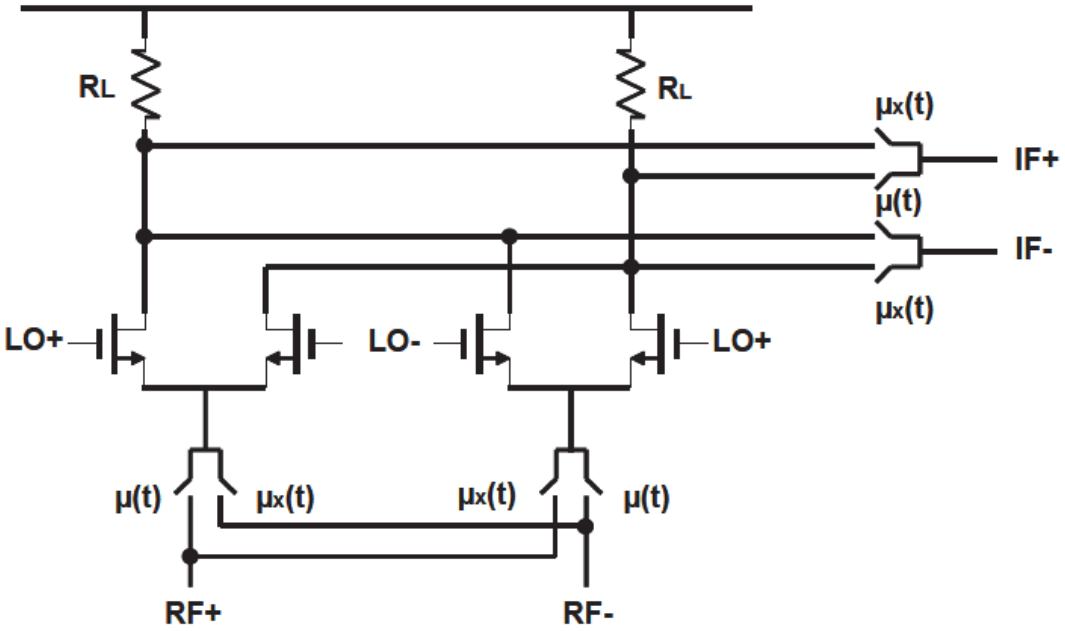
the whole implementation quite costly. Additionally, multiple inductors introduce undesirable cross-talk between distinct signal lines. When using strong LO signals to drive the mixer switches quickly (for instance in order to decrease their noise contribution), distortion sidebands around higher order harmonics are still demodulated to baseband without significant attenuation, lowering the effectiveness of the proposed technique.

3.3.3 Dynamic Matching

The concept of dynamic matching for direct downconversion mixers has been introduced in [55] and patented in [56]. The idea, shown in figure 3.7(a) [55], is equivalent to chopper stabilization technique, which has been successfully used to combat DC offsets and low frequency noise in operational amplifiers. Prior to downconversion with the LO signal, the input signal is multiplied with a mitigating signal μ(t) in a dynamic matching block. The mitigating signal can be either a periodic waveform or a pseudorandom signal. After the main mixing process, the second dynamic matching block restores the desired signal. The low frequency IMD2 distortion as well as static DC offsets generated in the main mixer are either frequency translated or spreaded, depending on the choice of the μ(t) waveform. In addition to reducing IMD2 distortion and static DC offsets, dynamic matching simultaneously reduces flicker (1/f) noise generated in the main mixer, making it an appealing solution especially for CMOS mixers.



(a) *Concept*



(b) *Implementation*

Figure 3.7 *Dynamic matching*

An example of dynamically matched mixer implementation is shown in figure 3.7 (b) [55]. Differential input signal in the current domain is mixed with the mitigating signal μ(t) using a double balanced switching mixer structure. Another double balanced structure is placed after the main mixing block (driven with the differential LO signal) and it restores the desired signal in the voltage domain.

Despite its valuable properties, dynamic matching possesses a number of drawbacks. First of all, mitigating signals generate interference at the fundamental frequency of μ(t) and its harmonics. Despite the fact that differential signaling, transmission line shielding and decoupling capacitors in signal buffers reduce on-chip crosstalk, taking the mitigating signals into account makes the whole design more complicated and consuming more power, which is a disadvantage by itself. Besides, although the LO and mitigation signals can be derived in a simple way from a single reference source by means of odd and even integer dividers (e.g. odd dividers used to generate mitigation signals while even dividers used for LO signal generation), such approach may result in mixing of even division multiple frequency component with odd division multiple frequency component causing a spurious response which self quiets the receiver. This deficiency has been pointed out in [57], which also suggests a solution to the problem: the use of mitigation signals with frequency having a non-integer relationship to the LO frequency (or the reference oscillator signal frequency). This can be accomplished for example with the help of a direct digital synthesizer (DDS) unit. However, it further increases the complexity of the whole system. Another weakness of dynamic matching is poor noise performance of the whole block, since each mitigating stage introduces loss associated with the mixing process. This amplifies the noise contribution of the following stages when referred to the input. Finally, dynamic matching units are also nonlinear and prone to mismatches. Their contribution to the overall even-order distortion can be lowered by implementing them as highly linear passive mixers and driving them with

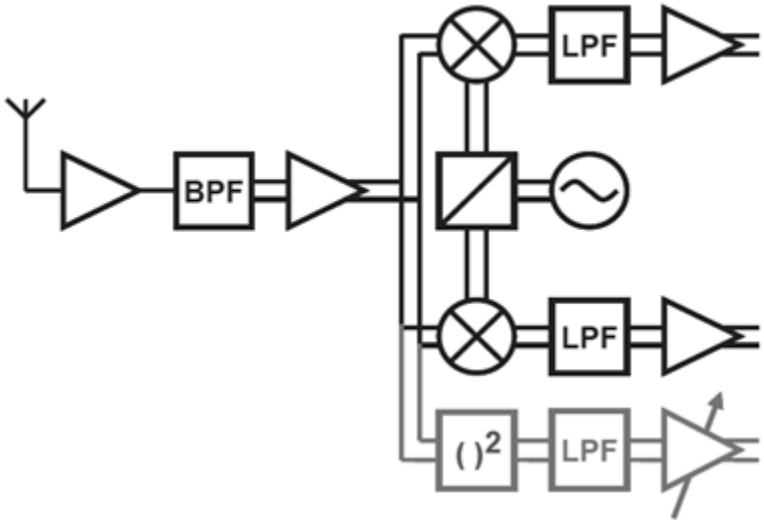
mitigation signals at low frequencies, where fast switching reduces the direct leakage while memory effects due to parasitic capacitances are less troublesome.

3.3.4 IMD2 Compensation

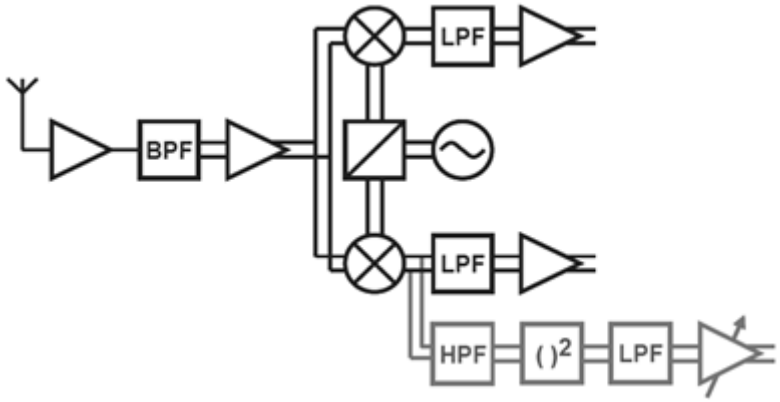
Instead of trying to eliminate sources of distortion, another approach is to try to eliminate the distortion itself [58]. This is where the idea of distortion compensation comes in. It can be loosely defined as addition of an out-of-phase, appropriately scaled distortion generated by a dedicated block featuring second order nonlinearity to the output signal of an RF block.

In case of downconversion mixers, input signals of the squaring block can be actually obtained either from the mixer input as shown in figure 3.8(a) as proposed in [59] or from the mixer output, before filtering of the interferers takes place, as shown in figure 3.8(b) and proposed in [60]. In the latter approach, a high pass filter removes the wanted signal while passing through the down-converted, out-of-channel interferers. Generally, separate gain settings are required for I and Q channels. The functions of the compensation system, including generation of reference distortion, scaling and subtraction can be carried out either in the analog or in the digital domain. When implemented in the analog domain, squaring operation can be performed by an instantaneous power detector. If implemented in the digital domain, squaring can be carried out by a dedicated multiplier. Since interfering signals are

relatively large, high resolution analog-to-digital converters in the reference path are not required. One more implementation is proposed in [61].



(a) *Reference signal obtained from the mixer input*



(b) *Reference signal obtained from the mixer output*

Figure 3.9 *Methods for reference signal generation*

Compensation techniques possess a number of drawbacks. First, they rely on accurate modeling of even-order nonlinearity of the RF block of interest. Since the modeling usually takes only second order distortion into account, compensation provides improvement for relatively small input

blocker levels while it fails at high input levels, where higher even order intermodulation terms become important. Next, compensation schemes require an additional path with its own set of filters, increasing the required area for on-chip integration. Moreover, an additional analog to digital converter is required if the compensation is to be carried out using digital techniques. In addition, extra equalization is required for matching of main path and auxiliary path, which in turn increase the complexity of the whole system.

3.3.5 Calibration Techniques

Instead of generating reference distortion by an additional block, it is possible to exploit common-mode distortion generated by existing circuit nonlinearities. Called calibration method, such self-compensating technique alters the RF block of interest by controlled tuning of component parameters in order to convert part of common mode distortion to differential mode. Since no additional active circuitry generating reference distortion is necessary, considerable savings in power consumption are possible. Moreover, the problem of modeling accuracy of the RF block nonlinearity is eliminated. For these reasons, calibration techniques are the most robust IMD2 cancellation techniques.

In [62], intentional mismatches were introduced between the biasing currents of the double-balanced harmonic mixer. In this way, operating points of the switching transistors were changed, affecting mismatches associated

with the indirect leakage and switching stage distortion. Although for such mixer the effective IMD2 mismatch is not exactly given, the idea is applicable also to standard Gilbert cell like mixers. In [63], a concept based on tuning the biasing voltages of both switching pairs separately was proposed. Therefore, values of mismatch coefficients associated with the first switching pair as well as the second switching pair could be decreased, cancelling simultaneously the impact of input stage transconductance mismatches. However, existence of other mismatches introduces undesirable ambiguity about which switching pair mismatch to tune in order to compensate for coupling or output stage imbalances. Similar tuning concepts were suggested in patents [64] and [65], suffering from the same drawbacks.

In [66], a remark was made that it is not necessary to change mismatches of both switching pairs separately. Accordingly, a technique based on introducing intentional mismatch in only one switching pair was proposed. Yet another approach to intentional mismatching of the switching stage by placing additional devices in parallel with the main switches was patented in [67]. The concept is more complicated than other IP2 tuning approaches described above. Moreover, it may degrade performance of the mixer because additional switches add their own parasitic capacitances loading the switching pairs.

In [68], calibration techniques for current mode output mixers were discussed, including input and switching stage mismatching. Although in the publication it was stated that introducing mismatch between linear

transconductances by tuning the biasing current flowing through each branch of the input stage has an impact on IIP2, it is strongly believed that in fact biasing current mismatching affects IIP2 much more through related switching stage mismatches than through input stage transconductance mismatches. Tuning circuits introducing mismatches in the output stage of the mixer can be divided into two groups: load resistance tuning circuits and common mode feedback loop mismatching circuits. In traditional voltage mode output mixers which don't employ output common mode feedback loops, controlling mismatches between the load resistors has proven effective. A so-called load balancing technique, which can be implemented by connecting a bank of large resistors in parallel to the main loads, was presented in [69] and patented in [70]. The second output stage IP2 tuning method introduces mismatches in the CMFB loop, provided that the mixer is equipped with such block. Variants of this technique were patented in [71] and [72] and also shown in [73] and [74].

3.3.6 Automatic IMD2 Cancellation

An important issue associated with above methods is how to appropriately scale the reference distortion (in case of IMD2 compensation) or adjust the settings of tuners (in case of calibration) so that the required suppression of second order intermodulation distortion is achieved.

Performing necessary adjustments as a part of post-production testing with the aid of dedicated measurement setups is not desirable for cost and

time reasons. A much more preferable solution is to let every fabricated receiver chip adjust itself automatically, without the help of external equipment. And this leads to development of automatic IMD2 cancellation techniques.

One of the first publications dealing with the subject of automatic IMD2 cancellation was [75]. The calibration settings were set based on measurements of received signal strength indicator (RSSI) and frame error rate (FER) for a specific communication system (PHS). Such approach is not advantageous for two reasons. First, it is a system dependent concept, requiring interaction with receiver blocks performing higher level system tasks including FER and RSSI measurements. Although technically feasible, this concept may be difficult to implement for organizational reasons since RF transceivers are usually developed independently from the baseband units. Secondly, the method presented in [75] is rather slow as signal level measurements take time and it may happen that they have to be performed for the whole range of tuning codes.

In [76], a general automatic calibration scheme was patented based on exciting the receiver with an AM modulated interferer having a known AM content and correlating the response with that AM content in order to determine necessary adjustments of one of the differential branches at the output of the down-converter. In another patent, supplying test tones and measuring the resulting DC offsets was proposed to determine the scaling

factor of compensating currents injected to the differential outputs of the mixer [77].

A technique based on reusing existing transceiver building blocks for generation of out-of band tones and AM modulating them using simple switches was proposed in [78]. The optimum IP2 tuner code was selected as the one corresponding to minimum interference level measured at the receiver output. Another method based on supplying an out-of-band test tone and detecting dynamic part of the output DC offset was presented in [79] and patented in [80] and [81].

3.3.7 Adaptive IMD2 Cancellation / Calibration

Adjustments of certain parameters in test signal based compensation and calibration schemes can be done only when the receiver is in idle mode, i.e. when it does not receive any desired signal. This happens for example just after power-up of the transceiver. However, it has been shown that the effective mixer mismatch varies with changes in operating conditions. For example, it depends on temperature, which changes rapidly after power-up. Thus, maintaining sufficient IMD2 suppression requires updating reference distortion gain coefficients (in case of IMD2 compensation schemes) or tuning codes (in case of calibration).

Such updates can be performed with test signals in a periodic manner. However, determination of when and how often to trigger the adjustment procedure requires careful planning on a system level. Moreover, in case of

wireless systems employing continuous transmission and reception, performing necessary adjustments periodically may be impossible. Thus, it is desirable to employ IMD2 cancellation techniques which are system independent and allow to keep satisfactory IMD2 suppression even with simultaneous reception of the desired signal. As a possible solution, statistical adaptive signal processing techniques can be utilized. Such methods have already proven useful in wireless receivers, for example in compensating static DC offsets and I/Q imbalances [37], [82], [83]. They are also an interesting option for IMD2 cancellation for a number of reasons.

The adaptive IMD2 compensation scheme was proposed in several publications. In [84], the reference signal was obtained by squaring the output signal of the mixer. For good cancellation of distortion, a multi-tap finite impulse response (FIR) equalizer was used, which combined the functions of scaling the amplitude of reference distortion and equalizing the main and reference signal paths. In [85], the reference second order distortion signal was obtained from the low-pass filtered output signal of the low-noise amplifier, thereby avoiding the use of a dedicated squaring block. However, the issue of nonlinear behavior of LNA and downconversion mixer at high input signal levels, where higher order distortion products start to play an important role, was not addressed. Publications [86] and [87] propose again the use of reference signal path, but apply it to cancel not only even order distortion but also odd order distortion. Other adaptive calibration techniques are proposed in [88-91].

3.3.8 Architectural Method

All the techniques discussed above can be classified in two categories. The first method uses an additional circuit for mixer non-linearity reduction. The second one uses an additional analogue or digital circuit for the IMD2 cancellation. Both solutions use dedicated software and hardware to reduce IMD2. The zero-IF receiver loses its advantages of high integration, simplicity and low cost by using these techniques. One possible solution is an architectural solution for distortion cancellation. One approach is to use five port architecture [92-94]. But, five port architecture consumes one more mixer and one more low-pass filter compared to conventional DCR. Therefore, use of five port receiver increases the component count and decreases the simplicity and compactness of the receiver. In this approach one more mixer will be added, which results in the addition of noise in the receiver. Other approach is to modified classical homodyne architecture [95].

3.4 I/Q mismatch reduction techniques

Gain and phase mismatch in the I and Q path will result in the I/Q mismatch problem. Gain error appears as a non unity scale factor in the amplitude, while phase imbalance corrupt one channel with a fraction of the data pulses in the other channel. This problem is a major obstacle in discrete designs, but it tends to decrease with higher levels of integration. Wireless devise for Cognitive – Radio (CR) application are very sensitive to this

problem. Therefore, major concentration has been put on the removal of this problem nowadays.

Solutions based on digital signal processing offer better accuracy, a higher degree of freedom and the possibility to compensate for several impairments while consuming less chip area.

Several techniques are proposed in the literature to solve the I/Q mismatch problem. These approaches can be classified in two broad categories as below.

3.4.1 Data - aided approaches

Data-aided approaches [96]–[102] rely on known pilot or training sequences in the transmitted signal for compensation. Thus these approaches are strongly-standard dependent.

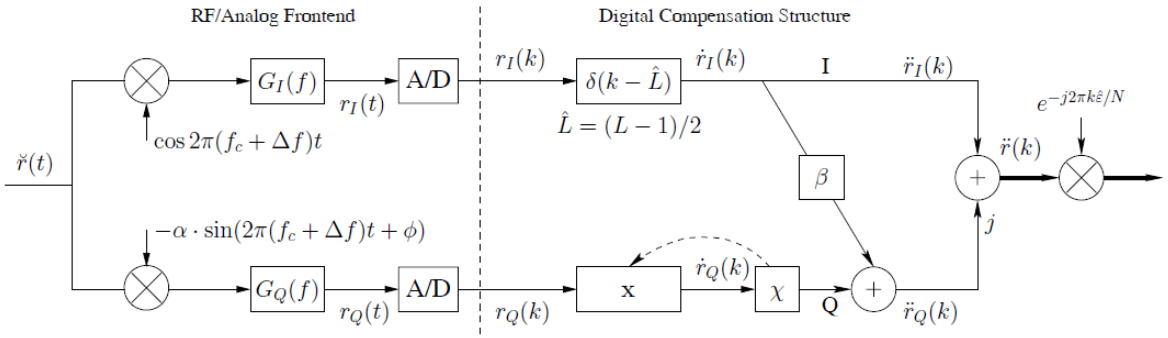


Figure 3.10 *Data-aided I/Q imbalance compensation in wideband DCR*

The received reference symbol contains the impairments of the entire signal processing chain in transmitter and receiver. Thus, such methods are suitable for the combined mitigation of several impairment sources. [96], [97]

compensate I/Q mismatch with least square approaches in combination with frequency offset as shown in figure 3., and [98], [99] together with channel estimation. [100] treats frequency dependent I/Q mismatch on the transmitter side and [101], [102] both on transmitter and receiver side in MIMO systems. With data-aided methods fast convergence and good performance are achieved, but often at the cost of high computational complexity, especially if considering compensation of frequency dependent I/Q mismatch.

3.4.2 Blind approaches

Blind methods [103-81] need longer convergence times but they are standard independent and thus are more flexible in its use. As changes of the I/Q mismatch due to temperature and aging appear slowly, convergence time is of less importance. Typically, blind methods rely on statistical properties of the influenced signal. As an example, [104] uses the statistical independence between the desired signal and its mirror image for frequency independent I/Q mismatch compensation in low-IF receiver by blind signal separation. Thus, such techniques can be used to selectively combat a single type of impairment. In OFDM-based systems the blind determination of the compensator coefficients in the receiver is possible before or after the FFT. In [105] a gradient descent search method in time domain and a frequency domain approach based on a single-tap matrix inversion for frequency dependent I/Q imbalance compensation is presented. [83] provides advanced blind source separation (BSS) techniques for frequency independent I/Q imbalance compensation in MIMO systems and [106] shows the same for the frequency

dependent case by using higher-order statistics (HOS) in an independent component analysis (ICA). A general feature of BSS techniques is their high implementation effort. A second-order statistical property which is destroyed by frequency dependent I/Q mismatch is properness, while in the frequency independent case it is called (second-order) circularity. It enables I/Q mismatch compensation algorithms in the time domain of the receiver in OFDM-based systems, which recover circularity [107-109] or properness [110-112] when the received signal is proper. The authors in [113-115] propose a Newton method based on a fourth-order moment for measuring frequency independent I/Q mismatch in communication signals used in LTE. This approach shows faster convergence speed compared with corresponding second order approaches. Compensation in the frequency domain [109], [113] can be realized only with significantly higher complexity, because the required statistics is subjected to a Fourier transformation. All of those blind I/Q mismatch compensation algorithms based on properness with complex signal models according to [110] are summarized in the following by the term complex-valued compensators (CVCs). In [116] such a CVC was introduced also on transmitter side for frequency dependent I/Q mismatch calibration. A realistic model for frequency dependent I/Q mismatch in currently used transceiver circuits is a finite impulse response (FIR)-filter with a few coefficients (typically 3-5) [117-118]. Less implementation effort can be achieved by using only real-valued filters for I/Q mismatch compensation according to [113], which we summarize under the term real-valued compensators (RVCs). The sensitivity of the objective function for I/Q

mismatch compensation algorithms with respect to other impairments needs to be taken into account for a practical implementation. [110],[119] examine the influence of several impairments on the properness. This properness property is efficiently utilized in [120]. Other I/Q imbalance estimation and removal methods are described in [121-123].

In conclusion, data-aided methods give fast convergence and good performance but at the cost of high computational complexity and dependency on standard utilized. Blind methods are standard independent and so give more flexible in its use, but need longer convergence times and sometimes high implementation effort.

3.5 Chapter Conclusion

All the above techniques are suffering from one or more of the below problems.

(i) Increase in the number of components in RF section.

(ii) Complex algorithm required to implement in the DSP section, results in the high computational loading.

(iii) Nullify only one distortion.

(iv) Required to modify the existing standard.

As a solution to these problems, an architectural approach has been adopted here to propose simple architectural solutions which nullify multiple

distortions simultaneously. Here a novel method with self calibration strategy is suggested to nullify multiple distortions in DCR. Self calibration method makes this approach standard independent and simple algorithm makes it fast and less computationally complex. Comprehensive simulated and practically measured results are presented to indicate the effectiveness of the proposed method.

Chapter 4

Analysis of Proposed Method for Distortion Reduction

4.1 General Consideration

Proposed method is based on the direct conversion receiver. Therefore analysis of classical direct conversion receiver is required for understanding of the proposed method and its distortion reduction ability. Next section describes the analysis of conventional DCR and then the analysis of proposed method is presented. Later in the chapter, distortion reduction ability of the proposed method is explained. At last the algorithm for computation of calibration coefficients is described.

4.2 Analysis of Classical DCR

A direct conversion receiver is shown in figure 4.1. Antenna receives the RF signal and apply that signal to the preselect filter for selection of the desired band.

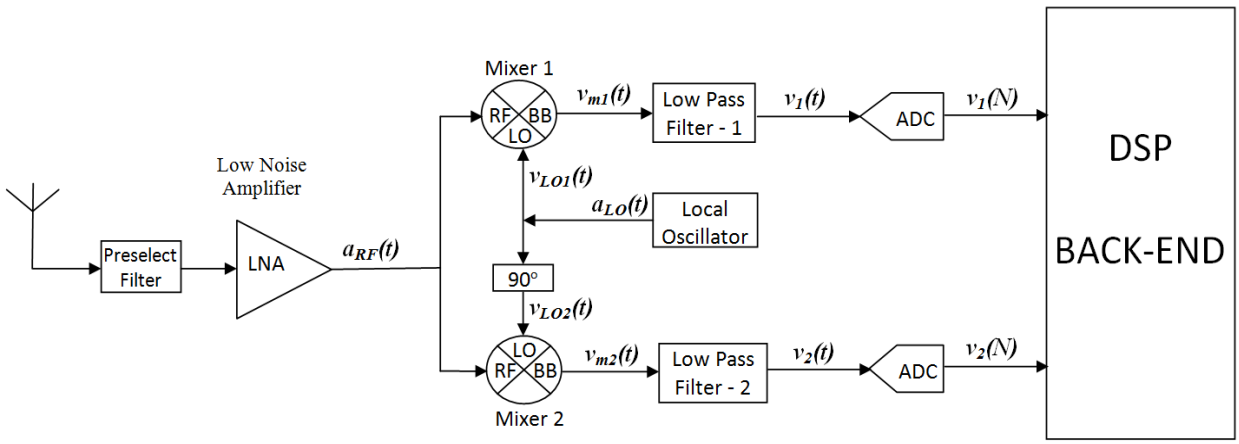


Figure 4.1 *Classical Direct Conversion Receiver*

It is important to distinguish between the band and the channel: the former includes the entire spectrum in which the users of a particular standard are allowed to communicate (e.g., the GSM receive band spans 935 MHz to 960 MHz), whereas the latter refers to the signal bandwidth of only one user in the system (e.g., 200 kHz in GSM)[8].

Preselect filter select the desired band signal and apply it to the low noise amplifier (LNA). Major functions of the LNA are (1) to amplify very weak RF signal, (2) as per "Friis formula", contribute minimum noise to maintain overall noise figure within limit. This amplified RF signal can be represented as $a_{RF}(t)$. This signal applied to both mixer-1 and mixer-2. Local oscillator (LO) generates the signal at the carrier frequency of the desired channel. This LO

signal is first shifted by 90^o and then applied to mixer-2, i.e. applied in quadrature phase to mixer-2, while LO signal is applied in-phase to mixer-1, i.e. without any phase change.

Function of mixer-1 is to beat RF signal with in-phase LO signal to generate in-phase component (I(t)) of the desired channel. While, function of mixer-2 is to beat RF signal with quadrature phase LO signal to generate quadrature component (Q(t)) of the desired channel. For this reason, mixer-1 is feed with in-phase while mixer-2 is feed with quadrature phase LO signal. Output of both mixers are filtered through low pass filter(LPF)s to select only the desired channel signal. The bandwidth of pass band of LPF is equal to the channel bandwidth, so that undesired signals can be removed to increase signal to noise ratio (SNR).

Output of LPF-1 and LPF-2 are digitized using analog to digital converter (ADC). These digitized I and Q signals are applied to digital signal processing (DSP) back-end section to extract I and Q data. Next we perform the mathematical analysis of direct conversion receiver.

A direct conversion receiver performs demodulation of a signal $a_{RF}(t)$ with carrier frequency f_{RF}, complex envelope $env(t) = I(t) + jQ(t)$, and amplitude A_{RF} using a signal $a_{LO}(t)$ generated by a local oscillator with frequency $f_{LO} = f_{RF}$ and amplitude A_{LO}. These signals can be represented by the two complex waves as (1) and (2).

$$a_{RF}(t) = A_{RF}(I(t) + jQ(t))exp(j2\pi f_{RF}t) \quad (1)$$

$a_{LO}(t) = A_{LO}\, exp(j2\pi f_{LO}t).$ (2)

The voltages $v_{RF}(t)$ and $v_{LO}(t)$ are obtained by taking the real part of (1) and (2)

$v_{RF}(t) = A_{RF}(I(t)cos(2\pi f_{RF}t) - Q(t)sin(2\pi f_{RF}t))$ (3)

$v_{LO}(t) = A_{LO}\, cos(2\pi f_{LO}t)$ (4)

$I(t)$ and $Q(t)$ represent the inphase and quadrature (I/Q) signals. The classical direct conversion receiver is presented in figure 4.1, which performs the demodulation of $v_{RF}(t)$. As shown in figure 4.1, RF signal input to mixer-1 and mixer-2 is $v_{RF}(t)$. While, local oscillator (LO) signal to mixer-1 is $v_{LO1}(t)$= $v_{LO}(t)$ and to mixer-2 is

$v_{LO2}(t)= A_{LO}\, cos(2\pi f_{LO}t+\pi/2)$ (5)

Output of low pass filter-1 is $v_1(t)$ and of low pass filter-2 is $v_2(t)$,

$v_1(t)= (A_{RF}A_{LO}/2).I(t)$ (6)

$v_2(t)= (A_{RF}A_{LO}/2).Q(t)$ (7)

$v_1(t)$ and $v_2(t)$ are converted in digital domain using analog to digital converter (ADC) and then applied to back-end digital signal processing (DSP) section to extract the transmitted data bits.

The critical function of the DCR is to extract the $I(t)$ and $Q(t)$ signal without distortion. Faithful reproduction of $I(t)$ and $Q(t)$ signals at receiver is greatly affected by distortions.

4.3 Proposed Method

The structure of proposed method for distortion removal is presented in figure 4.2.

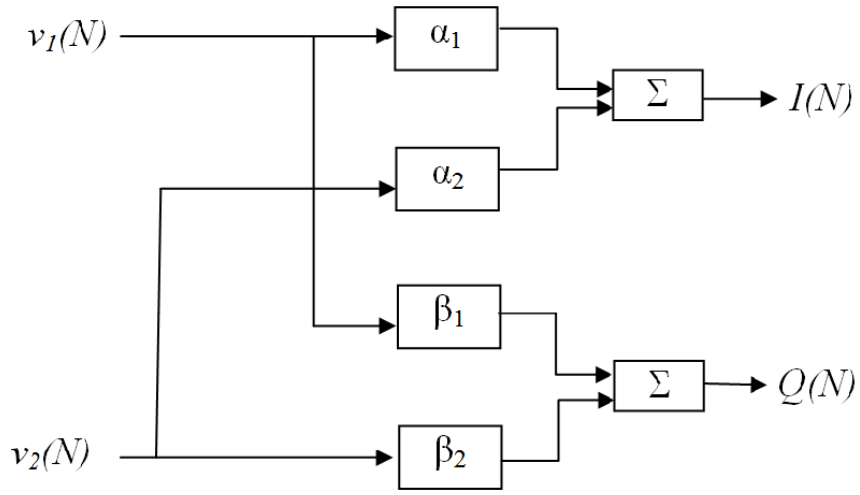


Figure 4.2 *Structure of proposed method*

In the proposed method multiplier and adder structure is utilized for reduction of distortion. In classical DCR $v_1(N)$ is itself I signal and $v_2(N)$ is Q signal. But in presence of distortion $v_1(N)$ and $v_2(N)$ are not original I and Q signal but they are distorted. As per the proposed structure of figure 4.2 the relation between sampled version of I and Q signals I(N) and Q(N) and $v_1(N)$ and $v_2(N)$ are

$$I(N) = \alpha_1 v_1(N) + \alpha_2 v_2(N) \quad (7\_a)$$

$$Q(N) = \beta_1 v_1(N) + \beta_2 v_2(N) \quad (7\_b)$$

The coefficients α_i , β_i are calculated in such a way that resultant signal I(N) and Q(N) are distortion free.

To reduce multiple distortions cascade version of multiplier and adder structure is utilized as shown in figure 4.3.

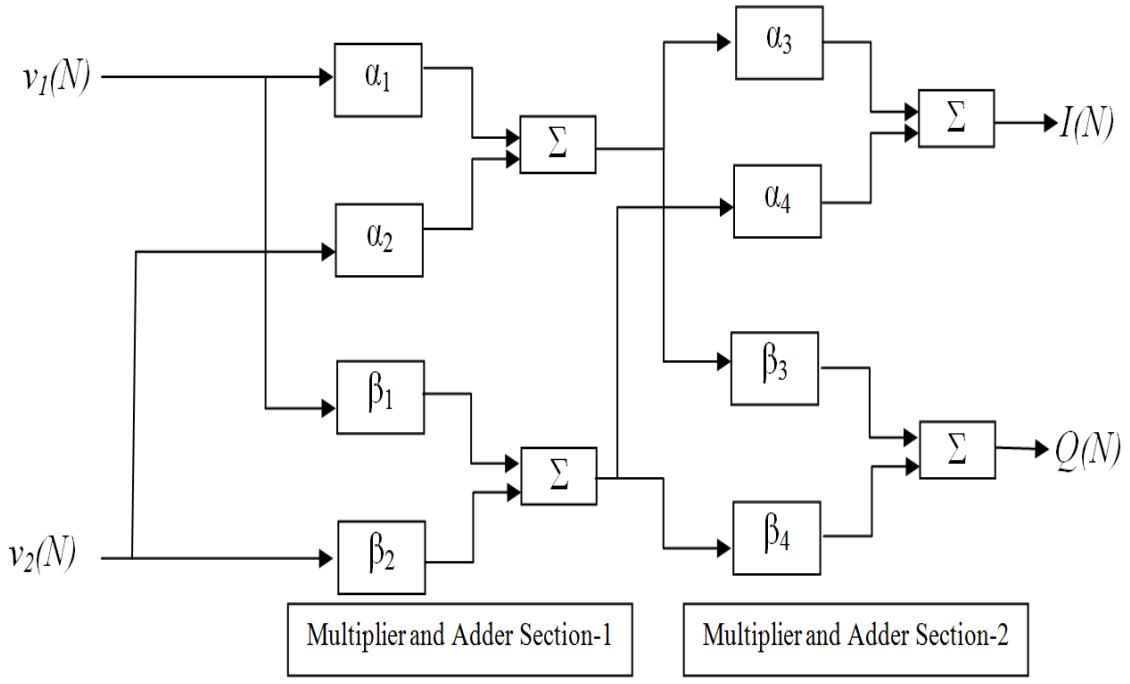


Figure 4.3 *Proposed method for multiple distortion removal (cascaded multiplier and adder structure)*

The multiplier constants or calibration coefficients α_i , β_i are calculated for suppression of particular type of distortion. As an example for the joint mitigation of I/Q mismatch and IMD2, multiplier and adder section-1 of figure 4.3 can be calibrated to remove IMD2 while multiplier and adder section-2 can be calibrated to remove I/Q mismatch or vice-versa. In reality cascaded structure can be replaced by single multiplier and adder structure as shown in figure 4.4 with relation,

$$\alpha_{1\_2} = \alpha_1\alpha_3 + \beta_1\alpha_4 \qquad (7\_c)$$

$$\alpha_{2\_2} = \alpha_2\alpha_3 + \beta_2\alpha_4 \qquad (7\_d)$$

$$\beta_{1\_2} = \alpha_1\beta_3 + \beta_1\beta_4 \qquad (7\_e)$$

$$\beta_{2\_2} = \alpha_2\beta_3 + \beta_2\beta_4 \qquad (7\_f)$$

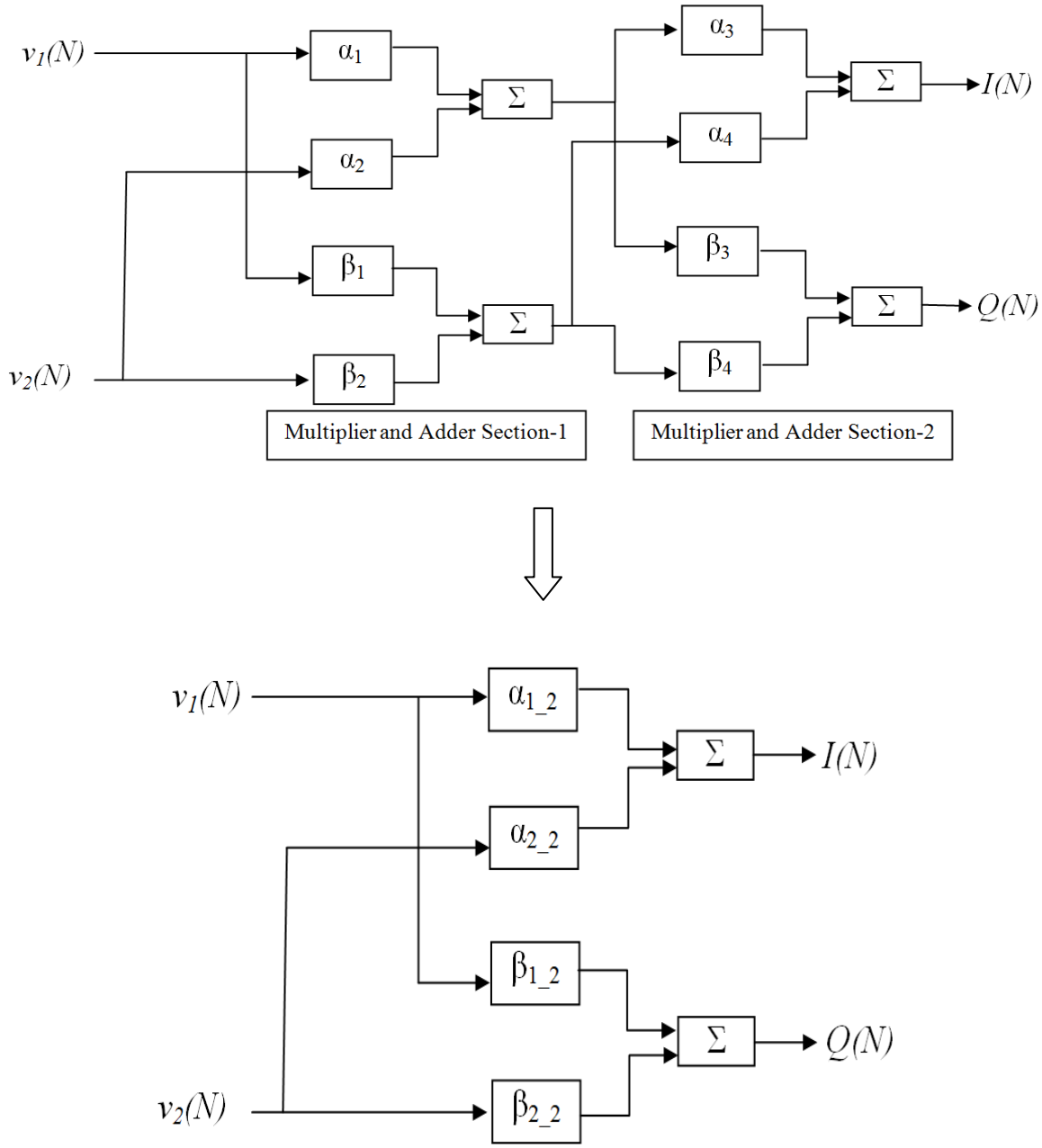


Figure 4.4 *Equivalency between single multiplier-adder section and cascaded multiplier and adder structure*

But in practice we implement cascaded structure because, algorithm used for calculation of calibration coefficients required knowledge of input as well intermediate signals. In addition, this structure is going to implement in DSP backend as shown in figure 4.5. Therefore, either we use cascaded structure or its equivalent single structure, resources utilized are same.

4.4 Analysis of Proposed Method in the Presence of I/Q Mismatch

Here, a mathematical analysis is presented to justify that the proposed method is able to detect desired base band signal *I(t)* and *Q(t)* from the received RF signal. The proposed method is represented in figure 4.5.

Here, we introduce I/Q mismatch distortion and then demonstrate the ability of proposed method to nullify effect of distortion on the output of the receiver. I/Q mismatch is introduced by taking different gain and phase for the local oscillator path-1 and path-2. In this case the local oscillator signal to mixer-1 and mixer-2, respectively, are

$$v_{LO1}(t) = A_{LO1}\cos(2\pi f_{LO}t+\phi) \quad (8)$$

$$v_{LO2}(t) = A_{LO2}\cos(2\pi f_{LO}t+\pi/2+\varepsilon) \quad (9)$$

where ϕ is the phase shift between received signal and locally generated carrier signal, while ε is phase shift introduced due to non- similarity in design and other factors.

Therefore, the output of low pass filters in the presence of I/Q mismatch are

$$v_1(t)= A_1.\cos(\phi).I(t)+ A_1.\sin(\phi).Q(t) \quad (10)$$

$$v_2(t)= A_2.\cos(\varepsilon).I(t)+ A_2.\sin(\varepsilon).Q(t) \quad (11)$$

where, A_1 and A_2 are gain of the signals at the output of low pass filters 1 & 2 respectively.

Using (10) and (11) a system can be written as (12),

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = B.\begin{bmatrix} I(t) \\ Q(t) \end{bmatrix}, \quad \text{with} \quad B = \begin{bmatrix} A_1\cos(\phi) & A_1\sin(\phi) \\ A_2\cos(\varepsilon) & A_2\sin(\varepsilon) \end{bmatrix} \tag{12}$$

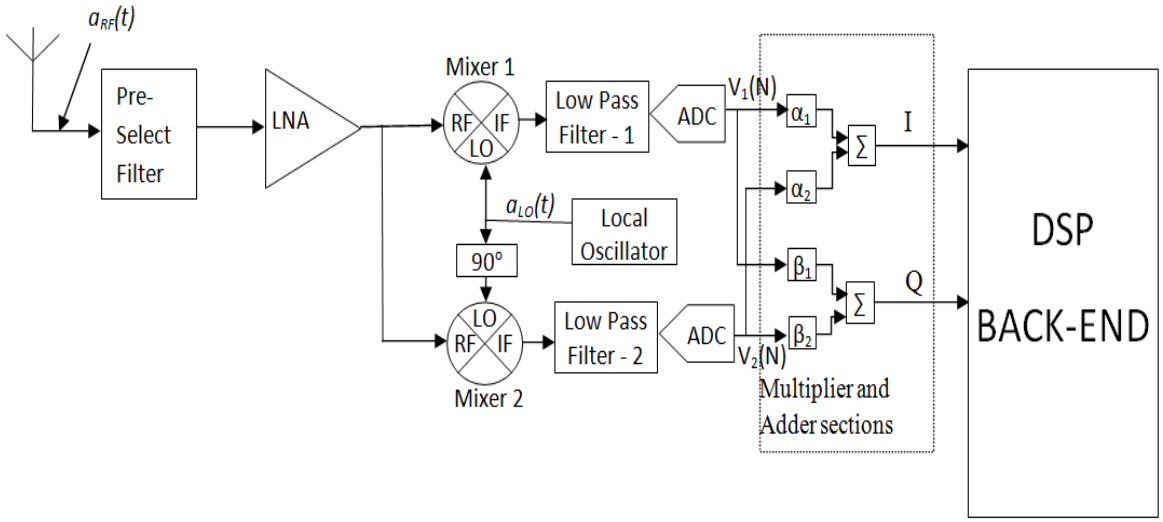


Figure 4.5 *Proposed Method for distortion removal in Direct Conversion Receiver*

If we suppose that the matrix B is nonsingular, then we obtain

$$\begin{bmatrix} I(t) \\ Q(t) \end{bmatrix} = B^{-1}.\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix}, \quad \text{with} \quad B^{-1} = \begin{bmatrix} \alpha_1 & \alpha_2 \\ \beta_1 & \beta_2 \end{bmatrix} \tag{13}$$

The expressions of the $I(t)$ and $Q(t)$ signals can be obtained with, (13) and the expression of the inverse of matrix B as,

$$I(t) = \alpha_1(v_1(t)) + \alpha_2(v_2(t)) \tag{14}$$

$$Q(t) = \beta_1(v_1(t)) + \beta_2(v_2(t)) \tag{15}$$

The relation between $I(t)$ and $Q(t)$ signals, the two output voltages $v_1(t)$, $v_2(t)$ and the four real calibration constants (α_1, α_2, β_1, β_2) is defined by equations (14) and (15). The calibration of the proposed method gives four real coefficients, which perform faithful I/Q regeneration from the two output voltages. The four calibration coefficients can be calculated using steps mentioned below.

1) An RF signal with known *I(t)* , *Q(t)* sequence (length of N symbols) is injected at input of the direct conversion receiver with proposed method. This input generates two output voltages $v_1(t)$ and $v_2(t)$ at the output port of low pass filters. These voltages can be used to write

$$C.\begin{bmatrix}\alpha_1\\ \alpha_2\end{bmatrix}=\begin{bmatrix}I(1)\\ \\ I(N)\end{bmatrix} \tag{16}$$

$$C.\begin{bmatrix}\beta_1\\ \beta_2\end{bmatrix}=\begin{bmatrix}Q(1)\\ \\ Q(N)\end{bmatrix} \tag{17}$$

with $C=\begin{bmatrix}v_1(1) & v_2(1)\\ \\ v_1(N) & v_2(N)\end{bmatrix}$

2) A deterministic least-square method can be utilized to calculate the four coefficients as

$$\begin{bmatrix}\alpha_1\\ \alpha_2\end{bmatrix}=(C^T.C)^{-1}.C^T.\begin{bmatrix}I(1)\\ \\ I(N)\end{bmatrix} \tag{18}$$

$$\begin{bmatrix}\beta_1\\ \beta_2\end{bmatrix}=(C^T.C)^{-1}.C^T.\begin{bmatrix}Q(1)\\ \\ Q(N)\end{bmatrix} \tag{19}$$

Thus, after determination of these four real coefficients, faithful I/Q regeneration can be performed. Proposed system can be calibrated using any one of the below mentioned methods.

1) Pre-calibration method: In this method, the four calibration coefficients are calculated during manufacturing process. For all the frequencies to be used, a known I/Q sequence is applied at the RF port of DCR and the calibration coefficients are stored in the memory.

2) Self-calibration method: Here a self calibration method is presented in figure 4.6. Advantage of this method is that it is standard independent and activated during the power-on process of the device or during the ideal/standby time duration. For explanation purpose the multiplier and adder blocks are represented separately, but usually they are part of the DSP back-end.

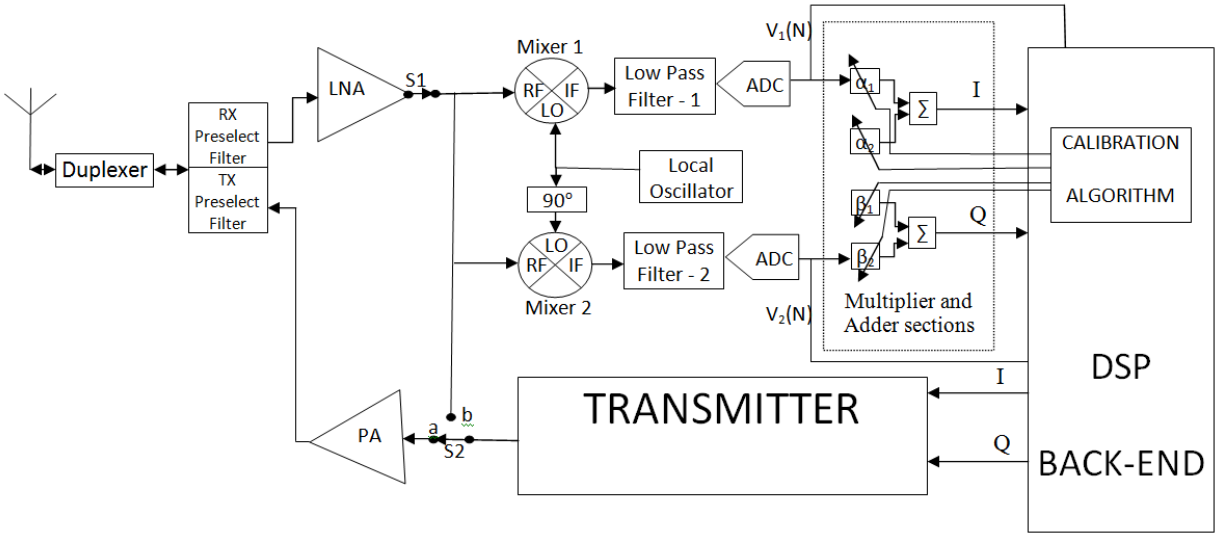


Figure 4.6 *Proposed method with self calibration*

When transceiver entered in the self calibration mode, switch S1 becomes open and switch S2 connected to terminal b, to bypass antenna section. DSP back-end section generates and applies *I(t)* and *Q(t)* sequences to Transmitter section. Transmitter section modulates the *I(t)* and *Q(t)* sequences and generates the RF signal. This RF signal is applied to receiver section. Receiver section down converts the received signal, low pass filters the signal and generates $v_1(t)$ and $v_2(t)$. $v_1(t)$ and $v_2(t)$ are converted in digital domain using analog to digital converter (ADC). These digitized signal $v_1(n)$ and $v_2(n)$, where n=1,...,N, are applied to calibration algorithm to calculate calibration coefficients α_i, β_i. Now, calculated calibration coefficients α_i, β_i are applied to

multiplier and adder section to perform error free regeneration of remaining *I(t)* and *Q(t)* samples.

4.4.1 Properties of Calibration Constants

For the precise understanding of the regeneration process of *I(t), Q(t),* the analysis of properties of calibration constants is required. Define the five following vectors.

$$V_o = \begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} \tag{20}$$

$$G_{\cos} = \begin{bmatrix} A_1.\cos(\phi) \\ A_2.\cos(\varepsilon) \end{bmatrix},\ G_{\sin} = \begin{bmatrix} A_1.\sin(\phi) \\ A_2.\sin(\varepsilon) \end{bmatrix} \tag{21}$$

$$\alpha = \begin{bmatrix} \alpha_1 \\ \alpha_2 \end{bmatrix},\ \beta = \begin{bmatrix} \beta_1 \\ \beta_2 \end{bmatrix} \tag{22}$$

The system defined by (10) and (11) becomes the vectorial relation

$$V_o = I(t)G_{\cos} + Q(t)G_{\sin} \tag{23}$$

Similarly, system defined by (14) and (15) becomes

$$I(t) = \alpha \cdot V_o \tag{24}$$

$$Q(t) = \beta \cdot V_o \tag{25}$$

By putting the expression of the vector V_o defined by (23) in (24), following relation for the *I* channel can be derived:

$$I(t) = I(t)\alpha \cdot G_{\cos} + Q(t)\alpha \cdot G_{\sin} \tag{26}$$

Therefore, the relations for the *I* channel can be expressed as:

$$\alpha \cdot G_{\sin} = 0 \tag{27}$$

$$\alpha \cdot G_{\cos} = 1. \tag{28}$$

Similarly, the relations for the Q channel can be expressed as:

$$\beta \cdot G_{\cos} = 0 \tag{29}$$

$$\beta \cdot G_{\sin} = 1. \tag{30}$$

From (27)-(30) following relations for the calibration procedure can be deduced:

1) The vectors α and β are, respectively, perpendicular to the vectors G_{sin} and G_{cos}, as per (27) and (29).

2) Equations (28) and (30) indicate that if A_i is low, the norms of vector α and β are high and vice versa.

4.5 Multiple Distortions Reduction Ability of Proposed Method

In a direct conversion receiver, pre-select filter (figure 4.5) suppresses the outband signals and allow the desired signal at frequency f_{LO} to be applied at the RF port of the direct conversion I/Q demodulator. In this situation, inband adjacent channel can pass through the preselect filter and makes its way to demodulator. In the direct conversion receiver, low-pass filters at output of the I/Q demodulator perform the task of channel selection. But, if the direct conversion receiver is suffering from second order intermodulation distortion (IMD2), then I and Q signals get distorted by a spurious baseband term produced by the adjacent channel signals [84]. We will study the joint effect of IMD2 and I/Q mismatch on the demodulation with the proposed method. Here the DC-offset due to self-mixing is removed by AC coupling

between mixer and low pass filter (LPF). This is possible, due to utilization of modulation scheme having very low power near to 0Hz i.e at DC. The proposed method for joint mitigation of IMD2 and I/Q mismatch, implemented in DSP back-end, is presented in figure 4.7. Here $v_1(N)$ and $v_2(N)$ are the signals respectively from ADC of LPF-1 and ADC of LPF-2. First multiplier and adder structure is utilized for IMD2 removal. The calibration algorithm for IMD2 removal take $v_1(N)$ and $v_2(N)$ signals as input and vary the coefficients α_1, α_2, β_1, β_2 in such a way that resultant signals $v_3(N)$ and $v_4(N)$ are IMD2 free. These $v_3(N)$ and $v_4(N)$ are feed as input signals to Calibration algorithm for I/Q mismatch removal. This calibration algorithm vary the coefficients α_3, α_4, β_3 and β_4 in such a way that resultant signals $v_3(N)$ and $v_4(N)$ are IMD2 and I/Q mismatch free. The algorithm for calculation of coefficients for I/Q mismatch removal is presented in section 4.4 and algorithm for calculation of coefficients for IMD2 removal is presented here.

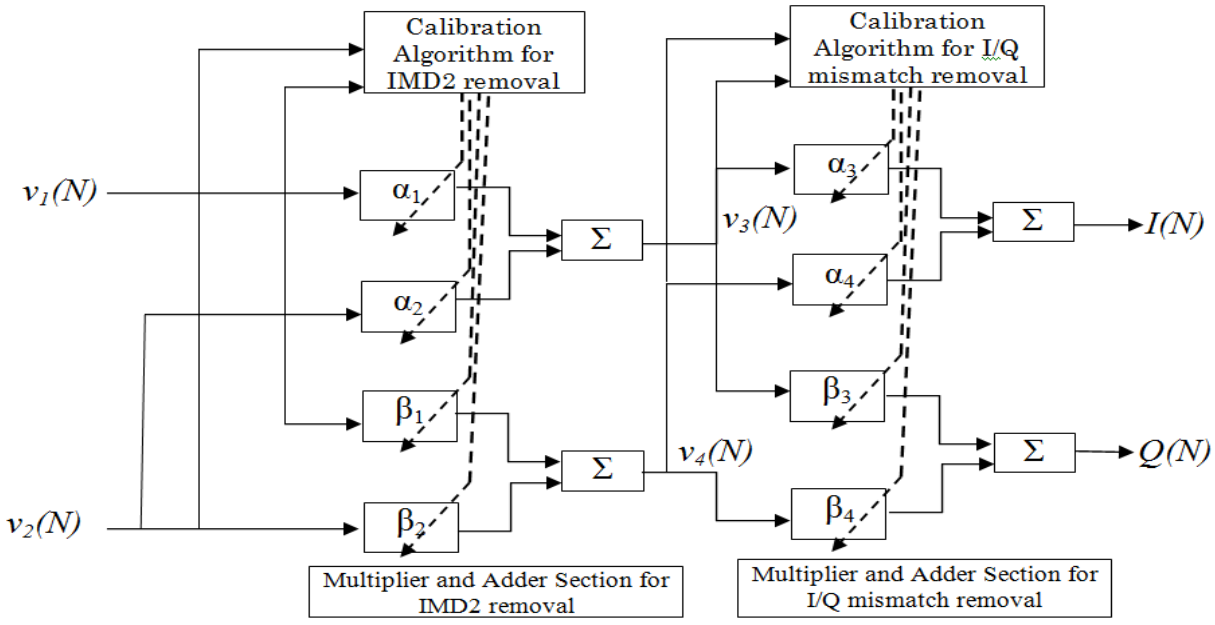


Figure 4.7 *Proposed method for multiple distortion removal*

With an adjacent channel present in the receiver reception frequency band, the input signal to the receiver is

$$a_{in}(t) = a_{RF}(t) + a_{adj}(t) \tag{31}$$

with $a_{adj}(t) = A_{adj}(I_{adj}(t) + jQ_{adj}(t))\exp(j2\pi f_{adj}t).$

The term $a_{adj}(t)$ represents the adjacent channel signal at frequency f_{adj}. The input voltages at the input of the demodulator is

$$v_{in}(t) = A_{Rf}(I(t)\cos(2\pi f_{RF}(t) - Q(t)\sin(2\pi f_{RF}t)) + A_{adj}(I_{adj}(t)\cos(2\pi f_{adj}t) - Q_{adj}(t)\sin(2\pi f_{adj}t)) \tag{32}$$

Using the down-conversion behaviour model given by [55], output of mixer-1 and mixer-2 can be expressed as

$$v_{m1}(t) = v_{in}(t).v_{LO1}(t) + \gamma_1\{v_{in}(t).v_{LO1}(t)\}^2 \tag{33}$$

$$v_{m2}(t) = v_{in}(t).v_{LO2}(t) + \gamma_2\{v_{in}(t).v_{LO2}(t)\}^2 \tag{34}$$

where, γ_i represents the second order transconductance of mixers. From (33) and (34) output of low pass filters are,

$$v_1(t) = A_1.\cos(\phi).I(t) + A_1.\sin(\phi).Q(t) + \gamma_1\{x_{RF}(t) + x_{adj}(t)\} \tag{35}$$

$$v_2(t) = A_2.\cos(\varepsilon).I(t) + A_2.\sin(\varepsilon).Q(t) + \gamma_2\{x_{RF}(t) + x_{adj}(t)\} \tag{36}$$

where, $x_{RF}(t)$ represents component of desired signal and $x_{adj}(t)$ represents component of adjacent channel.

Interference signal only affects the receiver when its power is much larger than that of the desired signal [92], i.e. $v_{Rf}(t) << v_{adj}(t)$, this implies that

$$x_{RF}(t) << x_{adj}(t) \tag{37}$$

Using this hypothesis, we can write (35) and (36) as

$$v_1(t) = A_1.\cos(\phi).I(t) + A_1.\sin(\phi).Q(t) + \gamma_1.x_{adj}(t) \tag{38}$$

$$v_2(t) = A_2.\cos(\varepsilon).I(t) + A_2.\sin(\varepsilon).Q(t) + \gamma_2.x_{adj}(t) \quad (39)$$

Using (14) and (15) with the output voltages defined by (38) and (39), the in-phase demodulated signal $\tilde{I}$ and the quadrature demodulated signal $\tilde{Q}$ can be expressed as:

$$\tilde{I} = \alpha_1.v_1(t) + \alpha_2 v_2(t) \quad (40)$$

$$\tilde{Q} = \beta_1.v_1(t) + \beta_2 v_2(t) \quad (41)$$

Assuming the system to be calibrated without the adjacent channel signal and by using the properties of calibration coefficients described in section 4.3, we obtain the two signals $\tilde{I}$ and $\tilde{Q}$,

$$\tilde{I} = I(t) + \left(\sum_{i=1}^{2} \alpha_i \gamma_i \right).x_{adj}(t) \quad (42)$$

$$\tilde{Q} = Q(t) + \left(\sum_{i=1}^{2} \beta_i \gamma_i \right).x_{adj}(t) \quad (43)$$

The calibration procedure allows the regeneration of I/Q signals, but does not remove the adjacent channel signal $v_{adj}(t)$. The response of the direct conversion receiver with proposed method at f_{RF} and f_{adj} are different, therefore the factors γ_i do not verify the relations (14) and (15). The desired signals [$I(t)$ and $Q(t)$] are corrupted by the adjacent channel. Next we describe a method to reject the effect of IMD2 and I/Q mismatch jointly.

4.5.1 Method for Joint Reduction of Distortions

Here, a method has been proposed that calibrates the system and rejects the effect of IMD2 and I/Q mismatch distortion jointly. A new vector

can be defined that consists of second order transconductance of mixers, as follow:

$$\gamma = \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \tag{44}$$

This vector corresponds to the adjacent channel. Using (21) and (44) in (38) and (39) we obtain the relation as follow:

$$V_o = x_{adj}(t)\gamma + I(t)G_{\cos} + Q(t)G_{\sin} \tag{45}$$

In order to reject the adjacent channel signal represented by $x_{adj}(t)$ and the vector γ, we propose the method of the projection of the vector V_o onto a plan H that is perpendicular to the vector γ. This concept is explained in the figure 4.8.

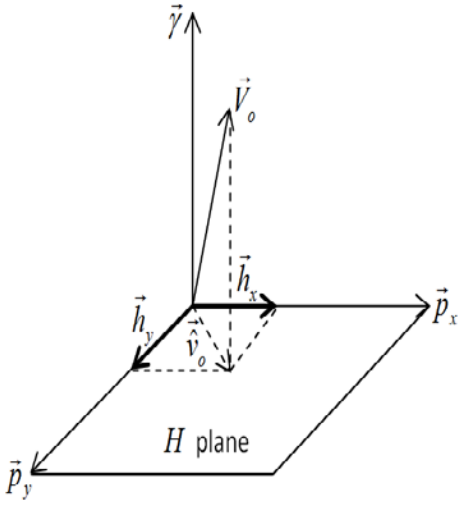


Figure 4.8 Vector *Diagram explaining removal of IMD2*

The plane H is defined by the orthogonal base $P = (p_x, p_y)$ with the following properties:

$$p_x \perp p_y, \quad p_x \perp \gamma, \quad p_y \perp \gamma. \tag{46}$$

The projection of the vector V_o onto the plane H can be defined using the following two scalar product:

$$h_x = V_o \cdot p_x \tag{47}$$

$$h_y = V_o \cdot p_y \tag{48}$$

Using (45) in (47) and (48) with the properties defined in (46), we get the following expressions:

$$h_x(t) = I(t)(p_x \cdot G_{\cos}) + Q(t)(p_x \cdot G_{\sin}) \tag{49}$$

$$h_y(t) = I(t)(p_y \cdot G_{\cos}) + Q(t)(p_y \cdot G_{\sin}) \tag{50}$$

We can see that the two projections h_x and h_y are independent of the adjacent channel signal. To calculate these projections, first we need to determine the base P. The vectors p_x and p_y can be determined as follows.

(1) Determine the coordinates of the vector γ.

(2) Construct a base P that verifies the properties defined by (46).

If the power of the adjacent channel signal is higher than the desired signal then and then, adjacent channel signal severely affect the performance of DCR. In this situation, the two output voltages are almost proportional to the term $x_{adj}(t)$, so we have the following approximation:

$$V_o \cong x_{adj}(t)\gamma. \tag{51}$$

In order to cancel the term $x_{adj}(t)$, we need to calculate the two standard deviations of the two output voltages using following expression

$$STD(v_i(t)) = \sqrt{\frac{1}{N}\sum_{l=1}^{N}(v_i(l) - \langle v_i(l)\rangle)^2}. \tag{52}$$

We obtain the two standard deviation values using N samples of output voltages (v_1, v_2), represented as below

$$V_{STD} = \begin{bmatrix} D_1 \\ D_2 \end{bmatrix} = \begin{bmatrix} STD(v_1(t)) \\ STD(v_2(t)) \end{bmatrix} \tag{53}$$

With, D_1 and D_2 representing the two elements of the vector V_{STD}. The vector V_{STD} is constant and proportional to the vector γ. Using (51), vector V_{STD} can be calculated as

$$V_{STD} = \begin{bmatrix} D_1 \\ D_2 \end{bmatrix} = STD(v_{adj}(t)) \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \tag{54}$$

With known elements of the vector V_{STD} , the base P can be constructed as

$$p_x = \begin{bmatrix} 1/D_1 \\ -1/D_2 \end{bmatrix}, p_y = \begin{bmatrix} D_1/(D_1^2 + D_2^2) \\ D_2/(D_1^2 + D_2^2) \end{bmatrix} \tag{55}$$

The vectors p_x and p_y shown above satisfy the properties defined by (46). The system of two equations (49) and (50) becomes the matrix relation

$$\begin{bmatrix} h_x(t) \\ h_y(t) \end{bmatrix} = E. \begin{bmatrix} I(t) \\ Q(t) \end{bmatrix} \tag{56}$$

with $E = \begin{bmatrix} p_x \cdot G_{\cos} & p_x \cdot G_{\sin} \\ p_y \cdot G_{\cos} & p_y \cdot G_{\sin} \end{bmatrix}$

Suppose that the matrix E is nonsingular, then

$$\begin{bmatrix} I(t) \\ Q(t) \end{bmatrix} = E^{-1}. \begin{bmatrix} h_x(t) \\ h_y(t) \end{bmatrix} \tag{57}$$

where $E^{-1} = \begin{bmatrix} s_1 & s_2 \\ u_1 & u_2 \end{bmatrix}$.

Using (57), the expressions of the $I(t)$ and $Q(t)$ signals are

$$I(t) = s_1 h_x(t) + s_2 h_y(t) \tag{58}$$

$$Q(t) = u_1 h_x(t) + u_2 h_y(t) \tag{59}$$

Equations (58) and (59) define the relation between *I(t)* and *Q(t)* signals, the two projections h_x and h_y, and the four real calibration constants (s_1, s_2, u_1, u_2). The calibration of the proposed method gives four real constants, which allow faithful *I/Q* regeneration from the two projections h_x and h_y voltages in the presence of second order intermodulation distortion. The method for the calculation of four calibration constants is as follows.

1) An RF signal with known *I(t)* , *Q(t)* sequence (length of N symbols) is applied at input of the direct conversion receiver, which generates two output voltages $v_1(t)$, $v_2(t)$ that can be used to find D_1 and D_2 using (52) and (53). D_1 and D_2 are utilized to calculate p_x and p_y using (55). p_x and p_y with $v_1(t)$, $v_2(t)$ are utilized to calculate h_x and h_y using (47) and (48). Using (58) and (59) these projection signals can be used to write

$$L.\begin{bmatrix} s_1 \\ s_2 \end{bmatrix} = \begin{bmatrix} I(1) \\ \\ I(N) \end{bmatrix} \tag{60}$$

$$L.\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} Q(1) \\ \\ Q(N) \end{bmatrix} \tag{61}$$

with $L = \begin{bmatrix} h_x(1) & h_y(1) \\ \\ h_x(N) & h_y(N) \end{bmatrix}$

2) The four constants can be calculated using the deterministic least-square approach as follows:

$$\begin{bmatrix} s_1 \\ s_2 \end{bmatrix} = (L^T.L)^{-1}.L^T.\begin{bmatrix} I(1) \\ \\ I(N) \end{bmatrix} \tag{62}$$

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = (L^T.L)^{-1}.L^T.\begin{bmatrix} Q(1) \\ \\ Q(N) \end{bmatrix} \tag{63}$$

Once these four real coefficients are determined, IMD2 and I/Q mismatch distortion free I/Q regeneration takes place using the two projection signals. The relation between s_1, s_2, u_1, u_2 and α_1, α_2, β_1, β_2 can be established as follows. Using (47), (48) and (55) the expressions of the $h_x(t)$ and $h_y(t)$ signals are

$$h_x(t) = \frac{v_1(t)}{D_1} - \frac{v_2(t)}{D_2} \tag{64}$$

$$h_y(t) = \frac{D_1.v_1(t)}{(D_1^2 + D_2^2)} + \frac{D_2.v_2(t)}{(D_1^2 + D_2^2)} \tag{65}$$

Therefore, the expressions of $I(t)$ and $Q(t)$ signals using (58), (59), (64) and (65) are

$$I(t) = \left[\frac{s_1}{D_1} + \frac{s_2.D_1}{(D_1^2 + D_2^2)}\right].v_1(t) + \left[\frac{s_2.D_2}{(D_1^2 + D_2^2)} - \frac{s_1}{D_2}\right].v_2(t) \tag{66}$$

$$Q(t) = \left[\frac{u_1}{D_1} + \frac{u_2.D_1}{(D_1^2 + D_2^2)}\right].v_1(t) + \left[\frac{u_2.D_2}{(D_1^2 + D_2^2)} - \frac{u_1}{D_2}\right].v_2(t) \tag{67}$$

By comparing (14) and (15) with (66) and (67) following relations can be established

$$\alpha_1 = \frac{s_1}{D_1} + \frac{s_2.D_1}{(D_1^2 + D_2^2)},\ \alpha_2 = \frac{s_2.D_2}{(D_1^2 + D_2^2)} - \frac{s_1}{D_2},\ \beta_1 = \frac{u_1}{D_1} + \frac{u_2.D_1}{(D_1^2 + D_2^2)},\ \beta_2 = \frac{u_2.D_2}{(D_1^2 + D_2^2)} - \frac{u_1}{D_2} \tag{68}$$

Equation (68) is only utilized when (51) is fulfilled. In the case when, (51) is not satisfied, (18) and (19) are utilized for calculation of calibration coefficients. Calibration algorithm decides which equations are to be utilized

on the basis of norm of h_x and norm of h_y. If condition (51) is satisfied the norm of h_x and norm of h_y are very low, otherwise norm of h_x and norm of h_y are high. A threshold is calculated as a part of calibration process to decide whether the norm of h_x and norm of h_y are low or high.

This method can also deal with multiple interferences. The detail mathematical analysis of the proposed method for multiple interference scenario is presented in appendix-A.

Chapter 5

Analysis and Measured Results of Proposed Method

Theoretical results need to be validated with the practical measurements. In first phase, a system is established in simulation environment to check the validity of the mathematical claim. After getting good results in simulation environment, a practical test bench is prepared for physical measurements of the various performance parameters. At last, obtained performance parameters are compared with the reported work till date. Comparison table is indicating that the proposed method is giving comparable performance with no extra hardware and very low computational loading. These results indicate that the receiver with proposed method can operate at high speed and consume low power.

5.1 Analysis & Results

5.1.1 Analysis

To validate these theoretical results, analysis using MATLAB-Simulink were performed. To model the non-linearity of the RF component, SimRF tool of Simulink is utilized. A snapshot of designed system model for analysis is shown in figure 5.1.

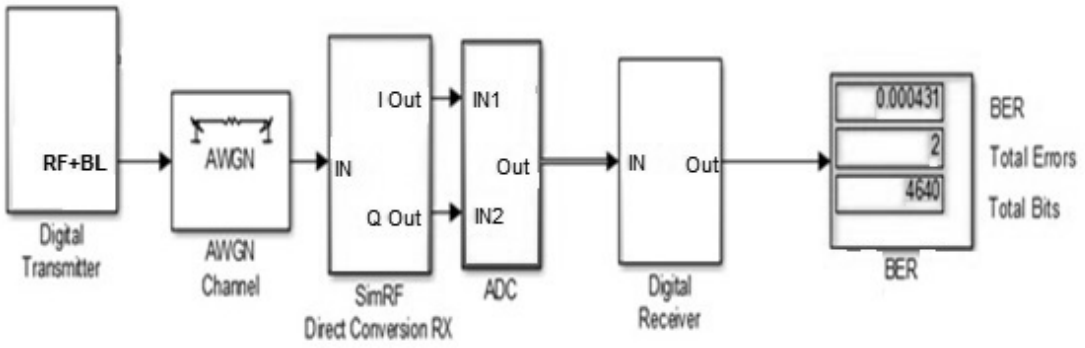
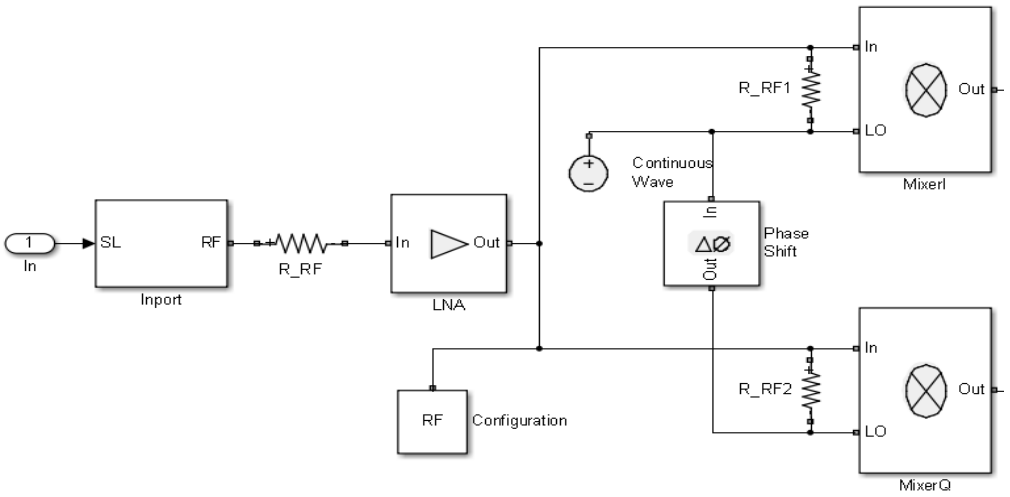


Figure 5.1 *Snapshot of system model utilized for analysis in MATLAB Simulink*

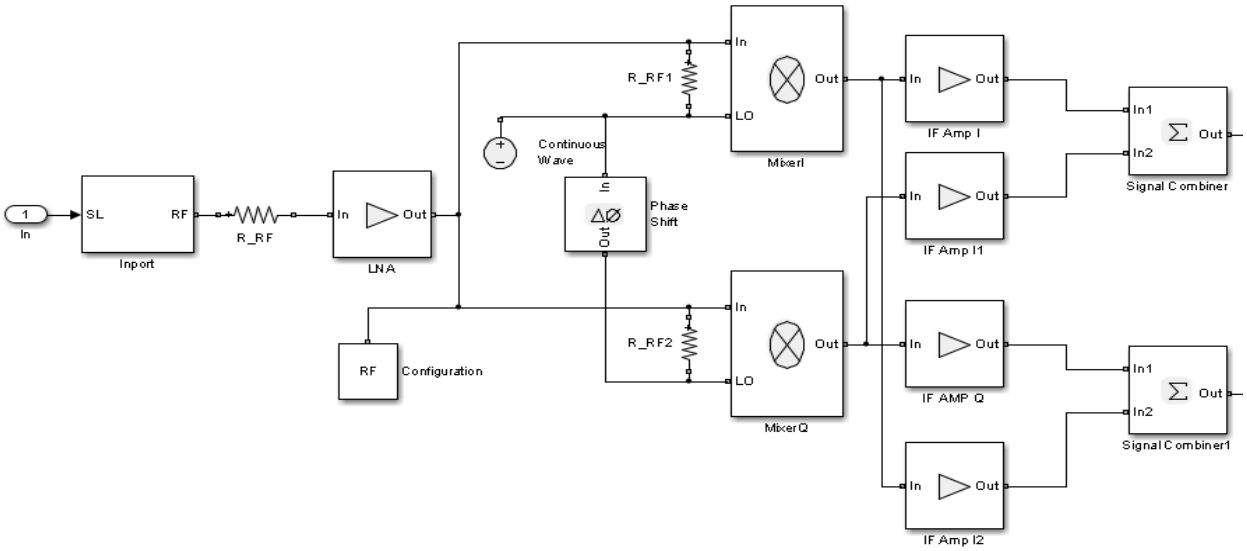
The digital transmitter consists of two QPSK modulator one for desired RF waveform, and another for interfering waveform. The waveforms are scaled and shifted in frequency for pass-band.

The direct-conversion RF receiver has a frequency conversion stage and two gain stages. Resistors model input and output impedances of the RF system as well as the isolation between the LO and RF ports of the mixers. The ADC block is utilized to convert continuous signal to discrete signal /

sampled signal. The digital receiver include algorithm for coefficients computation and also for bit-error-rate (BER) calculation.



(a) *Classical direct conversion receiver*



(b) *Proposed method*

Figure 5.2 *Simulated structure*

Each of the blocks captures RF impairments relevant to this design. Each of the nonlinear blocks is specified by noise figure. The LNA non-

linearity is specified by IIP3, and the nonlinearity in the intermediate amplifiers are specified by both IIP2 and IIP3. The mixer nonlinearity is specified by IIP2. A single LO and a phase shift block provide the cosine and sine terms to the I and Q branches, respectively. To model a thermal noise floor in the SimRF environment, the Temperature parameter in the configuration block specifies a noise temperature of 290.0 K. The SimRF system model utilized for classical homodyne architecture/ direct conversion receiver and proposed method is shown in figure 5.2(a) and (b).

The value of parameters taken in the simulation are based on [124] are given in table 5.1.

Table 5.1 *Test Parameters*

Block	Parameter	Value
Digital Transmitter/Receiver	Noise Temperature	293K
	Modulation Scheme	QPSK
	RF Frequency	2.400 GHz
	LO Frequency	2.400 GHz
	LO Power	13 dBm
	Blocker Frequency	2.403 GHz
LNA	Power gain	18 dB
	Noise Figure	3 dB
	Nonlinearity IP2	Infinite
	Nonlinearity IP3	10 dBm
Mixer	Power gain	10 dB
	Noise Figure	10 dB
	Nonlinearity IP2	7 dBm
	Nonlinearity IP3	Infinite
Power Level of Desired Signal		-55 dBm to -75 dBm
Power Level of Interfering Signal		-10 dBm to -70 dBm

5.1.2 Results

The simulation results are presented in figure 5.3 to 5.5. Figure 5.3 presents the effect of phase error between I(t) and Q(t) on the bit error rate (BER). Here the performance of classical DCR and proposed method are tested in the presence of phase error. Classical DCR architecture can maintain its performance for only low value of phase error i.e. upto 3^0-4^0. At the same time, proposed method can maintain its performance for large amount of phase-shift also. This indicates that the proposed method is insensitive to the phase shift error. Simulated constellation diagram for the classical DCR and proposed method is presented in figure 5.4(a) and (b) respectively. Constellation diagrams also demonstrate that the proposed method is insensitive to the I/Q mismatch.

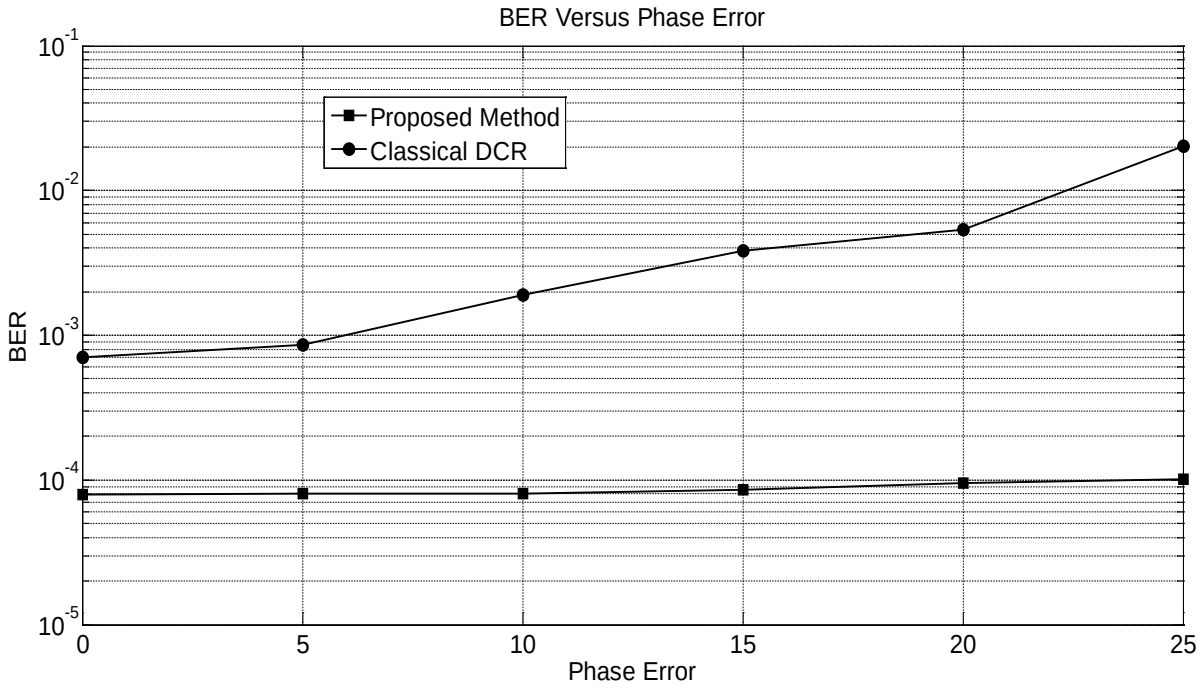
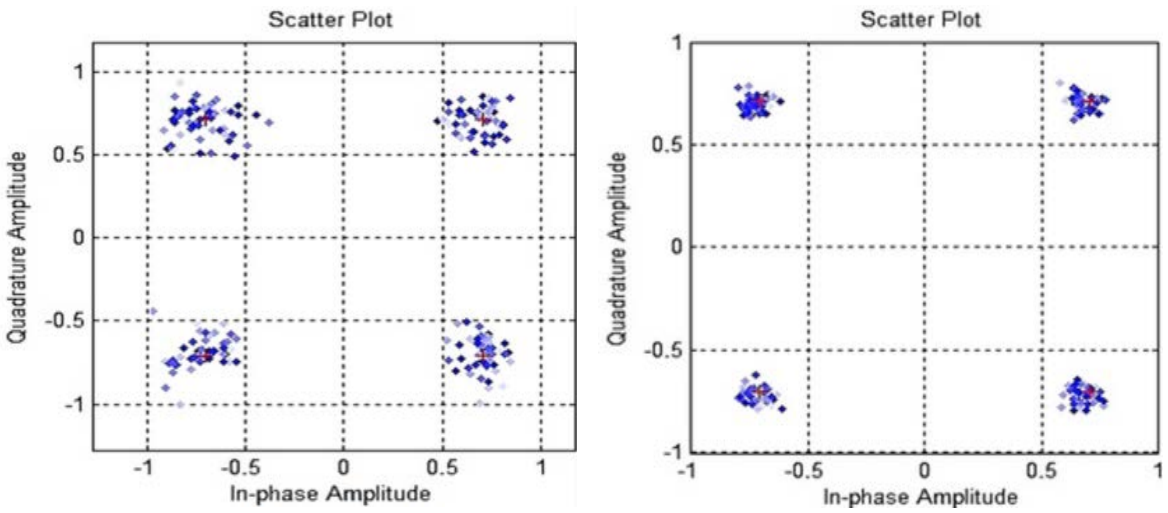


Figure 5.3 *BER versus Phase Error (degree)*



(a) *Classical DCR* (b) Proposed Method

Figure 5.4 *QPSK constellation*

Figure 5.5 shows performance of proposed method in the presence of DC-offset. DC-offset is implemented with the variation in LO to RF isolation. The value of isolation between RF port to LO port decides amount of leakage. Amount of leakage and value of isolation are inversely proportional. This leakage generates DC-offset, and results in the higher BER. As per the simulation result, the proposed method can tolerate quite large amount of DC-offset compared to classical receiver.

Proposed method is analytically tested for removal of I/Q mismatch and IMD2 distortion only. But practical result indicates that proposed method is able to suppress DC-offset distortions also. The explanation for this is as follows.

In proposed method, IMD2 effect is removed by projecting received signal on a plan which is perpendicular to the adjacent channel signal. The

resultant projection is free from adjacent channel signal. Adjacent channel signal also contribute to the DC-offset generation due to non-linearity of the mixer. Therefore, during the process of removal of adjacent channel signal, DC-offset generated due to adjacent channel also removed by the proposed method, which results into the reduction of total DC-offset, which in turn reduce the BER and improve the performance of the receiver. Thus, proposed method is also able to reduce DC-offset up-to some extent.

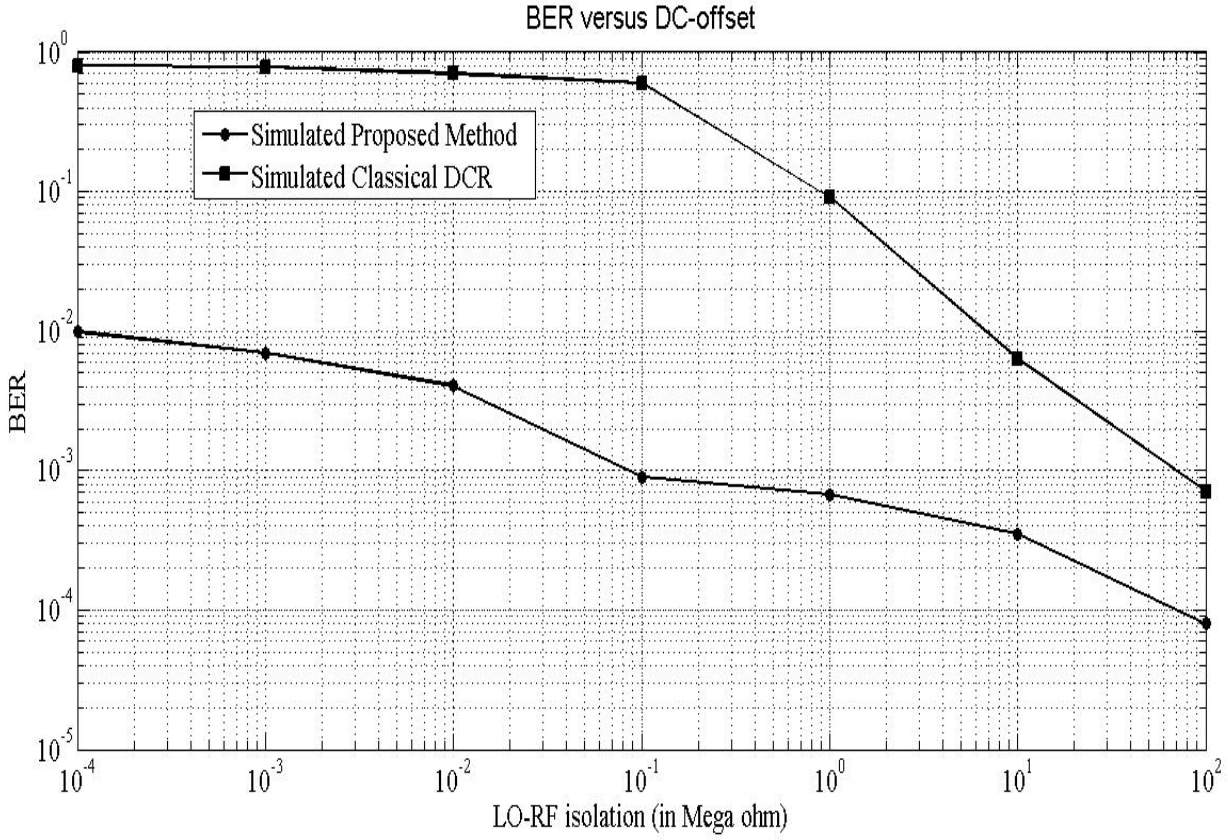


Figure 5.5 *BER versus LO-RF isolation (Mega Ohm)*

Other simulated results are jointly represented with the measured results in the next section.

5.2 Practical Test-bench Setup and Measurements

5.2.1 Practical Test-bench Setup

The test-bench utilized for experimental measurement is shown in figure 5.6. An RF signal at 2.4GHz with QPSK modulation is utilized. Out of the entire data sequence, first 16 symbols are utilized for training purpose (i.e. utilized for computation of co-efficients α_i and β_i). Remaining data symbols will be utilized for calculation of BER. The symbol rate utilized is 5 ksamples/s; thus RF QPSK modulated signal is at 10 kb/s.

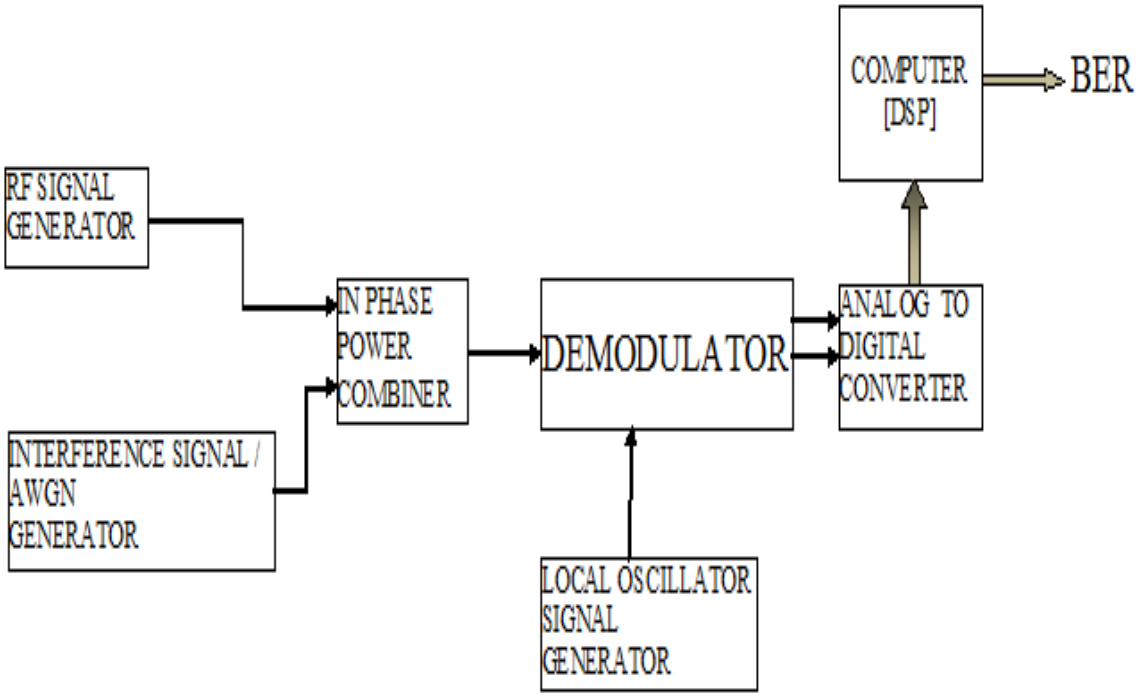


Figure 5.6 *Block-diagram of Practical Test-Bench setup*

The signal generator HM8135 (Hameg make) is the local oscillator tuned at 2.4GHz and the LO power is +10 dBm. The vector signal generator E44383 (Agilent make) generates the QPSK-modulated signal at 2.4GHz and the RF power is tuned according to the needs from -75 dBm to -55 dBm. Both generators are synchronized. One more signal generator utilized to generate an interfering signal or additive white Gaussian noise (AWGN) signal.

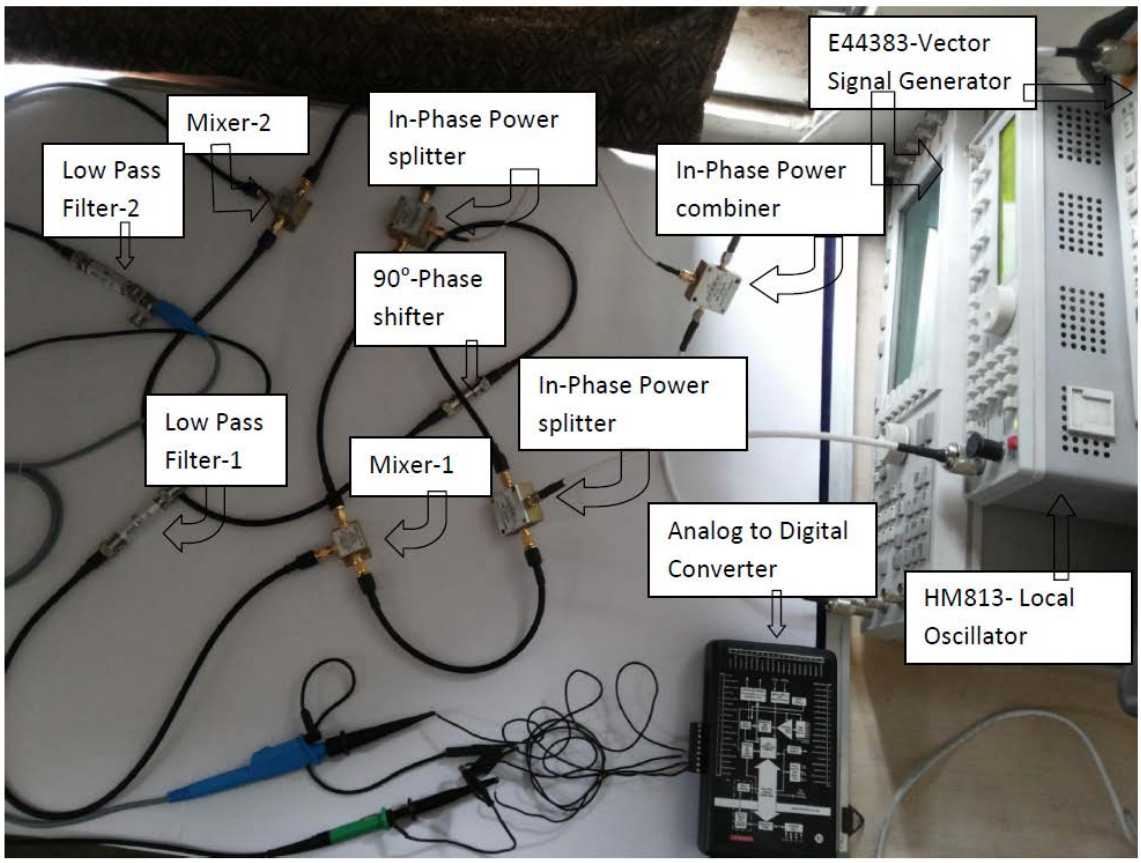


Figure 5.7 *Photograph of Practical Test-Bench setup*

The desired RF signal and interfering RF signal are added with a power combiner and applied to the RF input port of classical direct conversion receiver (DCR). The two down converted low-pass filtered output voltage of DCR are sampled by 16-bit Data Acquisition USB Module by KEITHLY and apply to the algorithm written in MATLAB for computation of coefficients α_i , β_i. All connecting cables are of equal length and equal loss. On base of the computed value of α_i and β_i demodulation of received sampled signal is done and then the received bits are compared with transmitted bits for computation of BER. We demodulate a large number of data sequence to estimate BER. A photograph of practical test-bench setup is shown in figure 5.7.

5.2.2 Measured Results

The practically measured results are presented in figure 5.8 to 5.11. First, we measure the performance of proposed method in the presence of Additive White Gaussian Noise (AWGN) only. RF signal and AWGN signal are combined with in-phase power combiner and then applied to the receiver input. Theoretically calculated bit error rate (BER) for QPSK system is compared with simulated and measured BER of classical direct conversion receiver as well as the receiver with proposed method of I/Q regeneration. As shown in figure 5.8, at BER = 10^{-3}, the value of Eb/No for theoretical curve is 6.8dB, for Measured proposed method is 7.6dB and for Measured classical DCR is approx. 8.8dB. Therefore, the implementation loss for DCR with proposed method is equal to 0.8dB, while for classical DCR it is approximately 2dB. Therefore the proposed method is more effective than the classical DCR.

Next sensitivity measurement (also known as quality of receiver) of the receiver is carried out. Sensitivity is the minimum RF input power required to ensure required BER. For this measurement, interference generator and power combiner have been removed from the set-up.

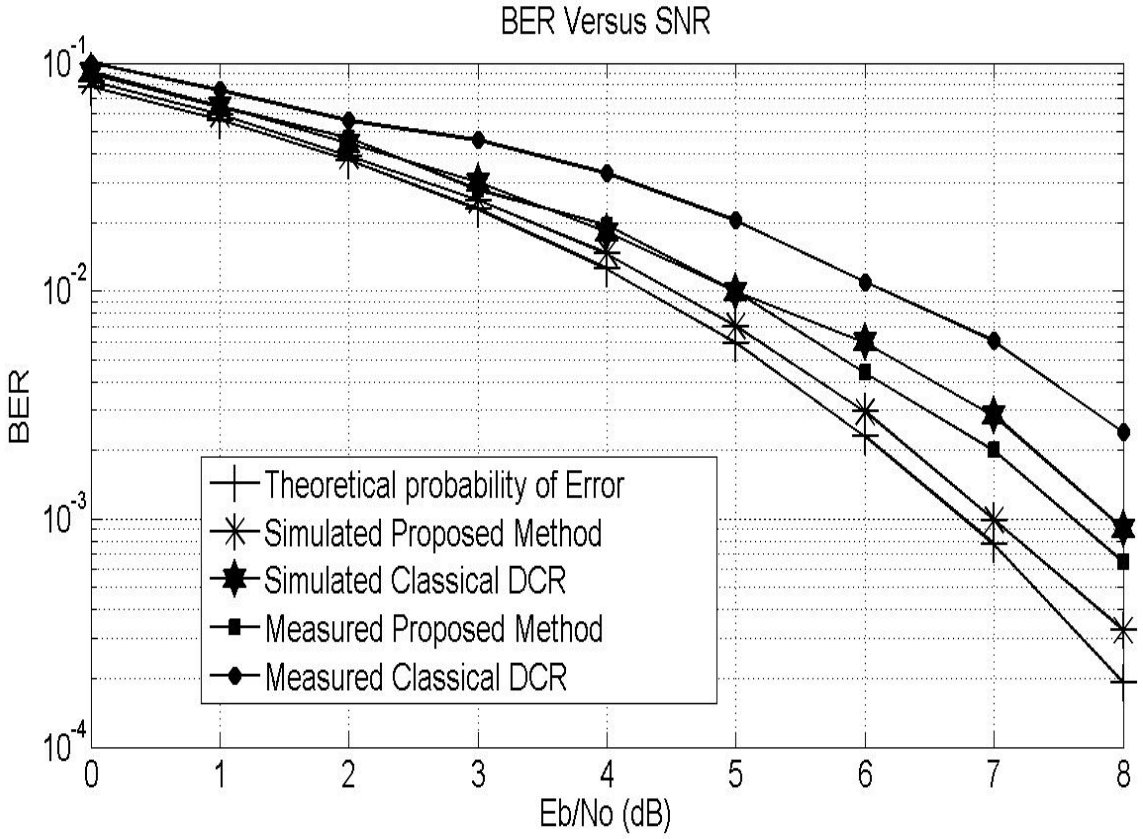


Figure 5.8 *BER versus SNR*

Figure 5.9 presents the sensitivity measurement of the receiver. This figure compares the quality of the classical DCR against DCR with proposed method. If required BER is assumed to 10^{-3}, then the measured sensitivity of proposed method is -62.5dBm, while that of classical DCR is -60.8dBm. In our test-bench, the quantization noise of A/D converter limits the sensitivity of the receiver, which can be alleviated by using a low-noise amplifier before the A/D

converter, or using the A/D converter with higher accuracy. The proposed method improves the sensitivity of the receiver by 1.7dB.

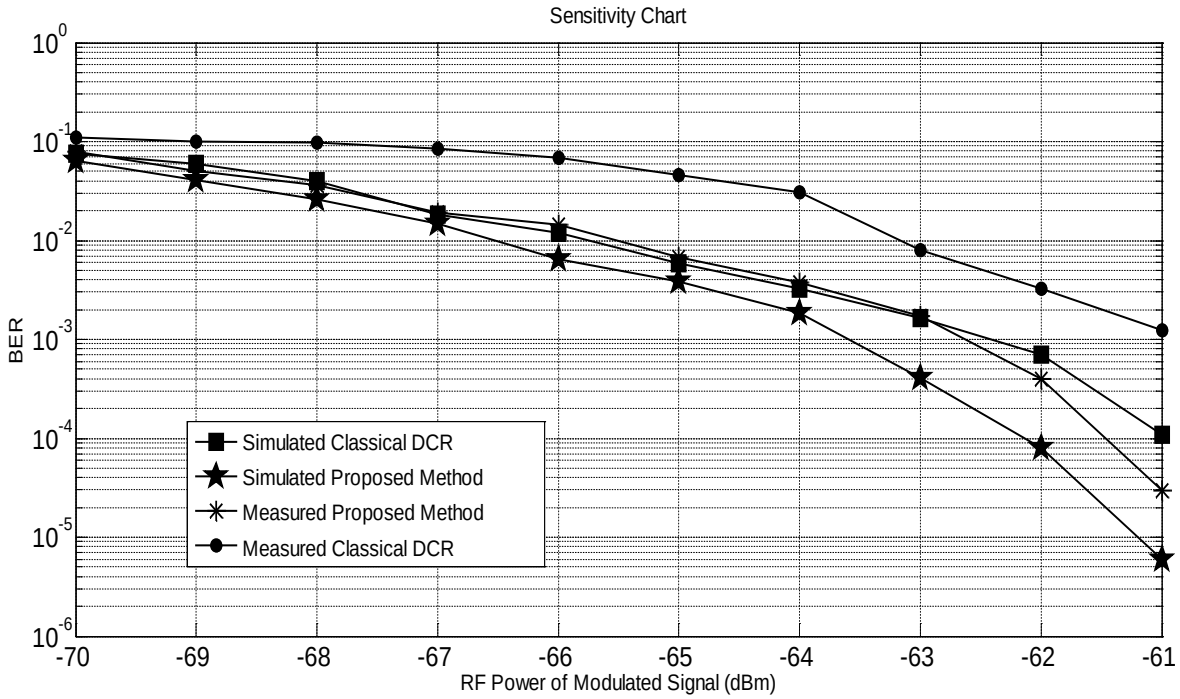
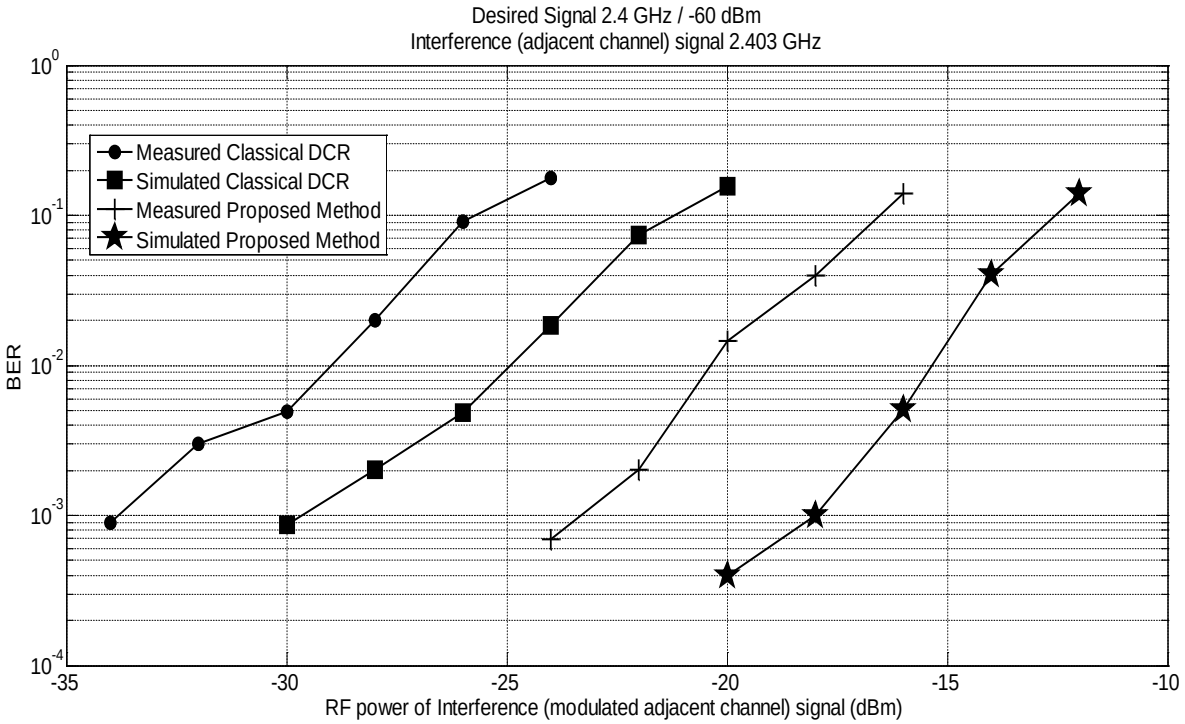


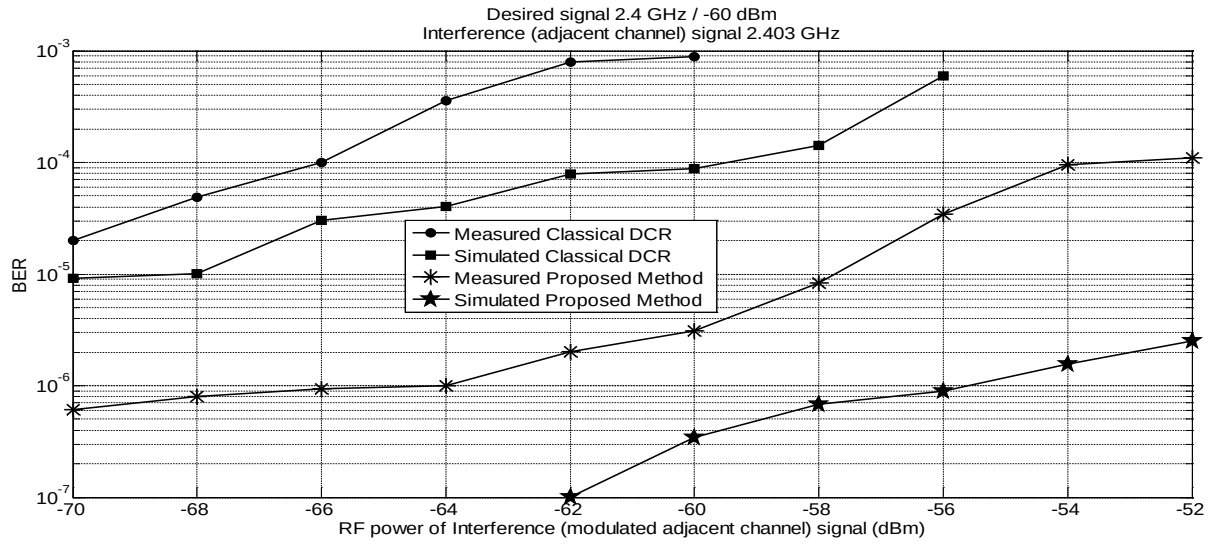
Figure 5.9 *BER versus RF power of signal*

Now we measure the performance of the proposed method with an interfering signal/adjacent channel signal. First, an interfering signal at 2.403 GHz has been combined with the desired signal at 2.4 GHz with RF power of -60dBm. Simulated and measured results are represented in figure 5.10 (a) & (b). Figure 5.10(a) presents the performance of the proposed method when equation (51), section 4.4 is satisfied i.e. the interference signal power is too large compared to desired signal power and method outlined in section 4.4, is utilized for regeneration of I/Q signal. These curves represent the ability of the receiver to reject the interfering signal using the proposed method. Interfering signal rejection ratio / Adjacent channel rejection ratio (ACRR) is defined as

the difference between the powers of the interfering signal and the desired signal to ensure that BER=10^{-3}. Interfering signal (adjacent channel) rejection for proposed method is 47dB and it is better than the classical receiver by 10dB.



(a) *Signal power << Interference power*



(b) *Signal power ≈ Interference power*

Figure 5.10 *BER versus Interfering signal power*

Figure 5.10(b) presents the performance of the proposed method when equation (51) is not satisfied i.e. interference signal power is not too large compared to desired signal power. When the norms of h_x and h_y reach to upper threshold limit, I/Q regeneration algorithm switch over to the method outlined in section 4.3. In figure 5.10(b), the curve of measured proposed method represents that as the norms of h_x and h_y are approaching to upper threshold limit, rate of decrease of BER is reducing. This indicates that the method outlined in section 4.4 is not effective when condition stated in equation (51) is not satisfied. But after the method changeover, the rate of decrease of BER is again increasing, which indicates that the method outlined in section 4.3 is effective when condition stated in equation (51) is not satisfied.

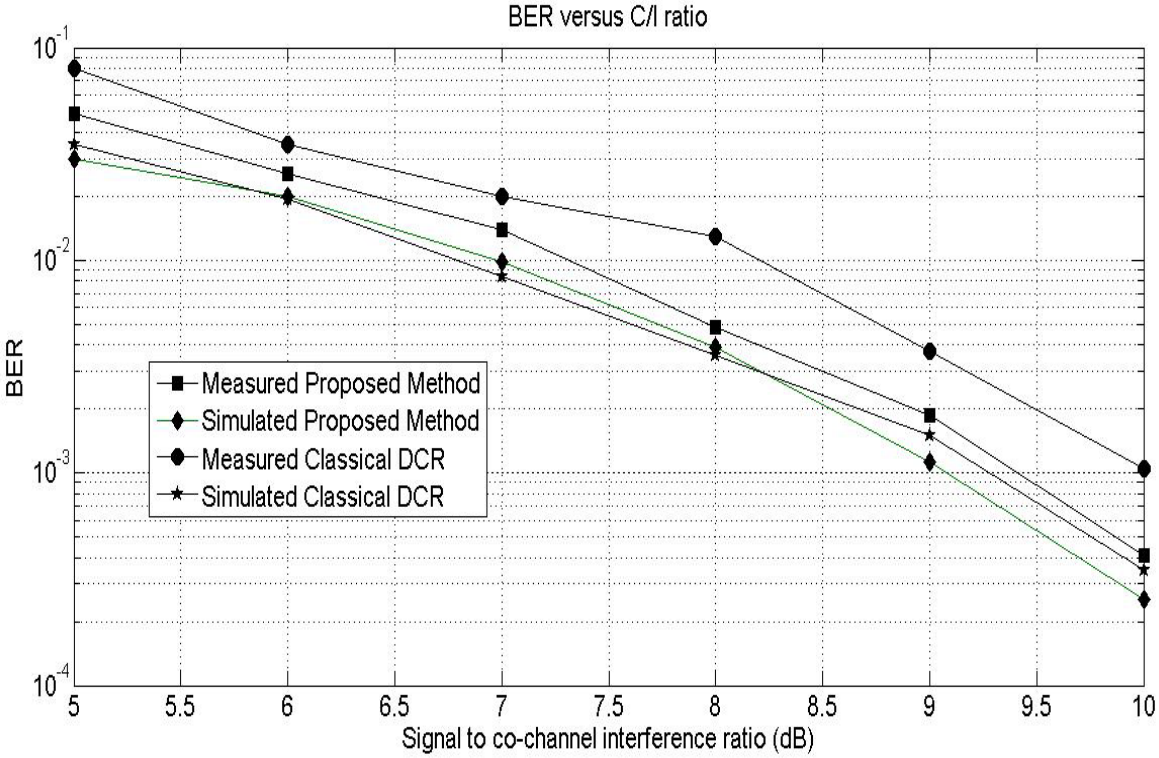


Figure 5.11 *BER versus signal to co-channel interference ratio*

Figure 5.11 shows BER measurements with co-channel interference. In the presence of a co-channel signal, the two output voltages are corrupted by a base-band term corresponding to the mixing between the local oscillator and the co-channel interferer. The C/I ratio is equal to 9.4dB at BER=10^{-3} for proposed structure.

Chapter 6

Conclusions and Discussion

6.1 Conclusions

In this thesis, various aspects of distortion in Direct Conversion Receiver (DCR) were investigated. Firstly, different types of receiver architectures are discussed with their strengths and weaknesses and it is shown that the DCR is the best choice for compact, low power and low cost design. Secondly, the importance of distortion in modern zero-IF receivers was stressed. An in-depth study of distortion in DCR was carried out using both behavioral and circuit level modeling techniques. Then, an overview of various distortion cancellation methods was given. Insufficiency of presented techniques for distortion suppression was indicated.

In the second part of the thesis, a novel method for homodyne receiver is presented, which is able to nullify the effect of distortions in DCR. Proposed method was designed to alleviate problem of I/Q mismatch and second order intermodulation (IMD2) distortions. But theoretical and experimental results

of the proposed method show its ability to suppress the DC-offset also. The proposed method is based on the classical homodyne receiver with two variable gain blocks and two adders. This added hardware can also be implemented in the DSP backend/ Digital signal processing section. Thus this structure does not add space for RF analog section on board. The gains of these two blocks are set in such a way that the final output is free from effect of distortion. The algorithm for computation of the gains is also illustrated. This algorithm does not need high computational complexity and can be easily implemented in DSP.

Experiments were then performed on the DCR with proposed method using QPSK signal to validate the presented theory. Measured results are in agreement with the presented theory. With reference to theoretical BER, proposed method with self calibration is having implementation loss of 0.8 dB. The sensitivity achieved with proposed method is -62.5 dBm at BER of 10^{-3}. The sensitivity of the proposed method can be further improved using Low Noise Amplifier (LNA), which is not utilized in the proposed test bench.

Here a self-calibration technique for the calibration of proposed method is also presented. This self calibration technique adapts calibration constants during the life of the system, rejects the distortion and regenerates the I/Q signals with minimum error. During the on-time period (or ideal period) the receiver can be entered in the calibration mode, during which the coefficients are computed to nullify the internal distortions of DCR. These calculated coefficients are then utilized to retrieve the data from the received signal. The

proposed method with self calibration does not require high computational complexity and can be easily implemented in DSP back-end section. This results into a cost-effective upgrading solution. This feature makes the proposed method very attractive. As the proposed method is very effective in distortion removal, a DCR with this robust, no extra hardware, distortion removal ability will be a good contender for IoT devices and cognitive radio receiver.

6.2 Discussion of Results

In this section, a comparison is made between this work and other previously reported work. A comparison table is shown in table 6.1.

A discussion on each comparison parameter is presented as follow:

1) Receiver Architecture: References [92-94] are using five-port based DCR which uses three mixers and three LPFs, while all other referred work and this work also, are using normal DCR architecture, which uses two mixers and two LPFs.

2) Types of Distortions Deal with: Reference [94] is dealing with three types of distortion (I/Q mismatch, IMD2, DC-offset), while this work is designed to deal with two types of distortion (I/Q mismatch, IMD2). But in simulation results, it is shown that, the proposed method is also able to deal with third distortion (DC-offset), while all other referred work dealt with only one type of distortion.

3) RF analog section-Hardware complexity: This parameter indicates the complexity / number of component in RF analog section. The work which utilizes only one LNA, two mixer and two LPFs is considered as a Reference structure. Depending on the number of components, other works are categorized in either LOW or HIGH complex structure.

4) Computational complexity: As the proposed method is implemented in the MATLAB, required hardware resources are not calculated. Hence, the comparison is done on the basis of number of mathematical operations. This parameter indicates HIGH if number of mathematical operations required is more than the operations required by proposed structure and otherwise indicate LOW.

5) BER @ SNR: This parameter indicates the value of SNR required to achieve BER of 10^{-3}.

6) BER @ P_{RF} level: This parameter indicates the value of P_{RF} (i.e. RF power) required to achieve BER of 10^{-3}.

7) Adjacent channel rejection ratio: This parameter indicates the value of adjacent channel rejection ratio achieved at BER of 10^{-3}.

Table 6.1 Comparison of proposed method with previously published work

Parameters For comparison	**[121]**	**[125]**	**[115]**	**[43]**	**[122]**	**[123]**	**[107]**	**[94]**	**[93]**	**[92]**	**This Work**
Receiver Architecture	DCR	DCR	DCR	DCR	DCR	DCR	DCR	Five-port DCR	Five-port DCR	Five-port DCR	DCR
Types of Distortion Deal with	I/Q mismatch	I/Q mismatch	I/Q mismatch	DC-Offset	I/Q mismatch, DC-offset	I/Q mismatch	I/Q mismatch	IMD2, I/Q mismatch, DC-offset	IMD2	IMD2	I/Q mismatch, IMD2, DC-offset
RF analog section hardware complexity	Equal	Equal	Equal	Equal	Equal	High	High	High	High	High	Reference
Computation-al complexity	High	N/A	High	High	High	High	High	Low	Low	Low	Reference
BER @ SNR	$6.6X10^{-3}$ @ 30dB Simulated	N/A	10^{-3} @ 37dB Simulated	10^{-3} @ 9.5dB Simulated	10^{-3} @ 22dB Simulated	10^{-3} @ 25dB Simulated	10^{-3} @ 17.5dB Simulated	N/A	N/A	10^{-3} @ 7.5dB Measured	10^{-3} @ 7.5dB Measured
BER @ P_{RF} level	N/A	$2.3X10^{-3}$ @ -3dBm Measured	N/A	N/A	N/A	N/A	N/A	10^{-3} @ -65 dBm Measured	10^{-3} @ -61 dBm Measured	10^{-3} @ -62.5 dBm Measured	10^{-3} @ -63 dBm Measured
Adjacent channel rejection ratio	N/A	N/A	N/A	N/A	N/A	N/A	N/A	45dB	37dB	35dB	47dB

From the tabular analysis, it can be concluded that the proposed method has comparable to good performance compared to previously reported work till date as per the best of my knowledge.

6.3 Suggestions for Further Work

In the course of research, some interesting areas of possible future study have been identified. Although distortion generation mechanisms have been thoroughly investigated, further research may include estimating the relative contribution of the low-noise amplifier nonlinearities to the distortion generation mechanisms, studying the impact of ground and power supply bounce on self-mixing as well as exploration of the impact of gate leakage current mismatches in ultra-deep submicron CMOS technologies on distortion in DCR. Additional studies could be carried out to investigate, dependence of distortions on multiple AM interferers widely spaced in the frequency domain.

Further research opportunities exist also in the area of distortion cancellation methods. Here proposed method is tested for only QPSK modulation scheme, but it can also be tested for other complex modulation schemes. This generalize distortion cancellation method opens up the possibilities of simultaneous cancellation of various other distortions. After finding the factors responsible for the distortions, the calibration algorithm can be modified to calibrate the coefficients to remove the effect of various distortions. Proposed method can be expanded in cascade structure with each stage alleviating one or more distortions. Then the impact of this cascaded

structure on the cost of hardware components, the impact of the increased power consumption on the battery life and other parameters need to be investigated.

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APPENDIX-A

Theoretical Analysis for Multiple Interference Scenario

Let input signal voltage to receiver in case of two adjacent channel interference is

$$v_{in}(t) = v_{RF}(t) + v_{a1}(t) + v_{a2}(t)$$

where,
$$\begin{aligned} v_{RF}(t) &= I(t)\cos\omega_{RF}(t) - Q(t)\sin\omega_{RF}(t), \\ v_{a1}(t) &= I_{a1}(t)\cos\omega_{a1}(t) - Q_{a1}(t)\sin\omega_{a1}(t), \\ v_{a2}(t) &= I_{a2}(t)\cos\omega_{a2}(t) - Q_{a2}(t)\sin\omega_{a2}(t). \end{aligned}$$

Let , local oscillator signal to mixer-1 is

$$v_{LO}(t) = \cos\omega_{LO}(t)$$

where, $\omega_{LO}(t) = \omega_{RF}(t)$

Output voltage of Mixer-1 is

$$v_{m1}(t) = v_{in}(t)v_{LO}(t) + \gamma_1\{v_{in}(t)v_{LO}(t)\}^2$$

$$v_{m1}(t) = v_{RF}(t)v_{LO}(t) + v_{a1}(t)v_{LO}(t) + v_{a2}(t)v_{LO}(t) + \gamma_1\{v_{RF}(t)v_{LO}(t) + (v_{a1}(t) + v_{a2}(t))v_{LO}(t)\}^2$$

$$\begin{aligned} v_{m1}(t) &= v_{RF}(t)v_{LO}(t) + v_{a1}(t)v_{LO}(t) + v_{a2}(t)v_{LO}(t) + \\ &\gamma_1\{v^2{}_{RF}(t)v^2{}_{LO}(t) + [v_{a1}(t)v_{LO}(t) + v_{a2}(t)v_{LO}(t)]^2 + 2v_{RF}(t)[v_{a1}(t) + v_{a2}(t)]v^2{}_{LO}(t)\} \end{aligned}$$

$$\begin{aligned} v_{m1}(t) &= v_{RF}(t)v_{LO}(t) + v_{a1}(t)v_{LO}(t) + v_{a2}(t)v_{LO}(t) + \\ &\gamma_1\left\{\begin{array}{l} v^2{}_{RF}(t)v^2{}_{LO}(t) + v^2{}_{a1}(t)v^2{}_{LO}(t) + v^2{}_{a2}(t)v^2{}_{LO}(t) + \\ 2v_{a1}(t)v_{a2}(t)v^2{}_{LO}(t) + 2v_{RF}(t)v_{a1}(t)v^2{}_{LO}(t) + 2v_{RF}(t)v_{a2}(t)v^2{}_{LO}(t) \end{array}\right\} \end{aligned}$$

The output of low pass filter – 1 (LPF-1) is

$$v_1(t) = LPF\{v_{m1}(t)\}$$

where, LPF{x} = low pass filtering of signal x.

$$\therefore v_1(t) = LPF\{v_{RF}(t)v_{LO}(t)\} + LPF\{v_{a1}(t)v_{LO}(t)\} + LPF\{v_{a2}(t)v_{LO}(t)\} +$$
$$\gamma_1\begin{Bmatrix} LPF\{v^2{}_{RF}(t)v^2{}_{LO}(t)\} + LPF\{v^2{}_{a1}(t)v^2{}_{LO}(t)\} + LPF\{v^2{}_{a2}(t)v^2{}_{LO}(t)\} + \\ LPF\{2v_{a1}(t)v_{a2}(t)v^2{}_{LO}(t)\} + LPF\{2v_{RF}(t)v_{a1}(t)v^2{}_{LO}(t)\} + LPF\{2v_{RF}(t)v_{a2}(t)v^2{}_{LO}(t)\} \end{Bmatrix}$$

Now we analyze each term separately,

$$LPF\{v_{RF}(t)v_{LO}(t)\} = I(t),$$

$$LPF\{v_{a1}(t)v_{LO}(t)\} = 0,$$

$$LPF\{v_{a2}(t)v_{LO}(t)\} = 0,$$

$$LPF\{v^2{}_{RF}(t)v^2{}_{LO}(t)\} = I(t)^2 + Q(t)^2 = \text{power or component of desired signal},$$

$$LPF\{v^2{}_{a1}(t)v^2{}_{LO}(t)\} = I_{a1}(t)^2 + Q_{a1}(t)^2 = \text{power or component of adjacent channel signal},$$

$$LPF\{v^2{}_{a2}(t)v^2{}_{LO}(t)\} = I_{a2}(t)^2 + Q_{a2}(t)^2 = \text{power or component of adjacent channel signal},$$

$$LPF\{2v_{a1}(t)v_{a2}(t)v^2{}_{LO}(t)\} = LPF\begin{Bmatrix} 2[I_{a1}(t)\cos\omega_{a1}(t) - Q_{a1}(t)\sin\omega_{a1}(t)] \\ [I_{a2}(t)\cos\omega_{a2}(t) - Q_{a2}(t)\sin\omega_{a2}(t)][\cos\omega_{LO}(t)]^2 \end{Bmatrix}$$

$$LPF\{2v_{a1}(t)v_{a2}(t)v^2{}_{LO}(t)\} =$$
$$LPF\begin{Bmatrix} [I_{a1}(t)I_{a2}(t)\cos\omega_{a1}(t)\cos\omega_{a2}(t) - I_{a1}(t)Q_{a2}(t)\cos\omega_{a1}(t)\sin\omega_{a2}(t) - \\ Q_{a1}(t)I_{a2}(t)\sin\omega_{a1}(t)\cos\omega_{a2}(t) + Q_{a1}(t)Q_{a2}(t)\sin\omega_{a1}(t)\sin\omega_{a2}(t)][1+\cos 2\omega_{LO}(t)] \end{Bmatrix}$$

$$LPF\{2v_{a1}(t)v_{a2}(t)v^2{}_{LO}(t)\} = 0$$

Similarly,

$$LPF\{2v_{RF}(t)v_{a1}(t)v^2{}_{LO}(t)\} = 0$$

$$LPF\{2v_{RF}(t)v_{a2}(t)v^2{}_{LO}(t)\} = 0$$

Let,

$$LPF\{v^2{}_{RF}(t)v^2{}_{LO}(t)\} = I(t)^2 + Q(t)^2 = x_{RF}(t) \text{ and}$$
$$LPF\{v^2{}_{a1}(t)v^2{}_{LO}(t)\} + LPF\{v^2{}_{a2}(t)v^2{}_{LO}(t)\} = I_{a1}(t)^2 + Q_{a1}(t)^2 + I_{a2}(t)^2 + Q_{a2}(t)^2 = x_{adj}(t)$$

Therefore,

$$v_1(t) = LPF\{v_{m1}(t)\} = I(t) + \gamma_1\{x_{RF}(t) + x_{adj}(t)\}$$

This equation is same as the equation [eq. no (35)] of output of LPF-1 in the presence of single interference. Thus for n number of interference the output of LPF-1 would be of the above structure and therefore the proposed method is able to deal with multiple interferences.

List of Publications

1) Shah, Milind, and Gupta, Sanjeev, "Baseband I/Q regeneration Method for Direct Conversion Receiver to nullify effect of I/Q mismatch." Advanced Electromagnetics, vol.5, No.3, November 2016, pp. 50-55.

2) Shah, Milind, and Gupta, Sanjeev. "Baseband I/Q regeneration Method for Direct Conversion Receiver to nullify effect of Second Order Intermodulation Distortion" Accepted for publication in International Microwave and RF Conference (IMaRC 2017).

Patent Applied For

1) Shah, Milind, and Gupta, Sanjeev, "A Method for Reduction of Distortions in Direct Conversion Receiver (DCR)." Indian Patent No.: 201621022753, 01, July 2016. [Filed at Patent office, Intellectual Property India, Govt. of India]

Fellowship Awarded

Awarded prestigious "Inspire Fellowship" by the Department of Science and Technology (Govt. of India), on behalf of President of India, for pursuing my Ph.D. programme in the month of January, 2011.